Optoelectronic Assembly of a Silicon Photonic 4-Channel Coherent Receiver Array

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***Abstract*—A 4-channel IQ receiver array with individual optical inputs has been fully packaged in an optoelectronic assembly including an RF Rogers PCB, an Alumina PCB as fan-out and photonic wire bonds for optical coupling with fiber arrays. BER performance demonstrates potential 240Gbps aggregated data rate.**

Keywords—Integrated coherent optical receiver, silicon photonics, photonic wire bond.

I. Introduction

The increasingly massive use of services such as video streaming, social media and remote work applications, i.e. video conferencing and the use of virtual private networks (VPN), leads to a constant grow of inter- and intra-data center traffic. Scaling beyond PAM-4 seems only a matter of time, and adaptation of the short-reach data center interconnect to quadrature modulation offers an energy-efficient alternative to intensity-modulation/direct detection (IM/DD) links, therefore fostering the use of coherent detection as already happens for long-haul transmissions [1]. Novel power- and cost efficient approaches to coherent data- and telecom links are therefore of utmost importance, with integration of transceivers in compact modules taken for granted in case of data centers [2],[3]. In addition to numerous realizations based on heterogeneous integration between electronic and photonic integrated circuits, recent works realized silicon photonic coherent receivers monolithically co-integrating high-speed electronics [4],[5]. However, optical access through conventional grating couplers (GCs) limits the operational wavelength range to about 35–40 nm, requiring ad-hoc GCs either for the O- or for the C-band [5]. Here we present an optoelectronic assembly based on a silicon photonics 4-channel coherent optical receiver array, where the optical connections between silicon waveguides and fiber arrays (FAs) are realized through wavelength-independent photonic wire bonds (PWBs) [6]. The assembly includes a Rogers printed circuit board (PCB) to collect each receiver radiofrequency (RF) output and provide the direct-current (DC) control voltages/biases required by the silicon photonic integrated circuit (PIC). Two additional Alumina PCBs are also included as fan-out interposers for RF connections.

II. Assembly Description and Test

The packaged PIC layout is shown in Figure 1. Each channel of the coherent optical receiver array consists of a 90° optical hybrid with individual inputs (local oscillator LO, signal SIG) implemented by using three 2x2 MMI couplers with two thermal phase shifters (PSs) to finely tune the desired 90° phase shift, and a pair of 50 GHz balanced photodiodes (BPDs) as the I and Q outputs. Optical inputs of two channels are accessible on each PIC side (left, right) through both GCs and edge couplers. DC controls for PSs, BPD biases, and BPD RF outputs for two channels, are accessible through the

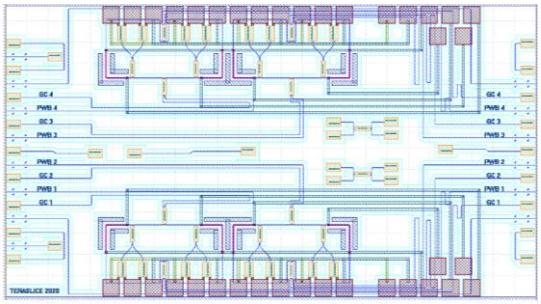

Figure 1. Mask layout of the realized coherent optical receiver

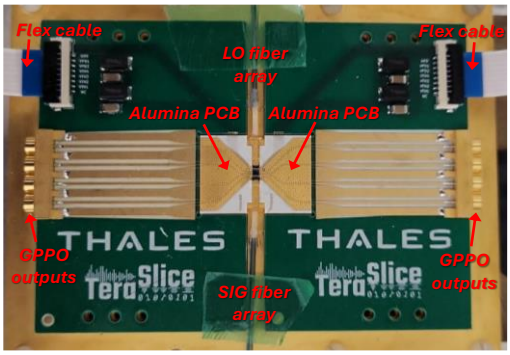

Figure 2 Picture of the assembly.

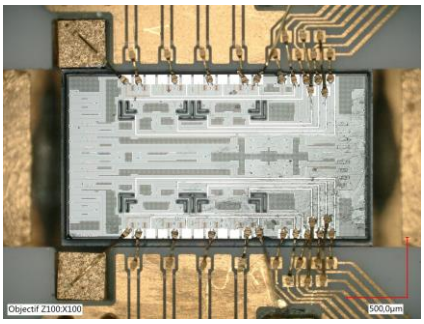

Figure 3 Zoom of the Alumina PCBs wedge-bonded to the PIC.

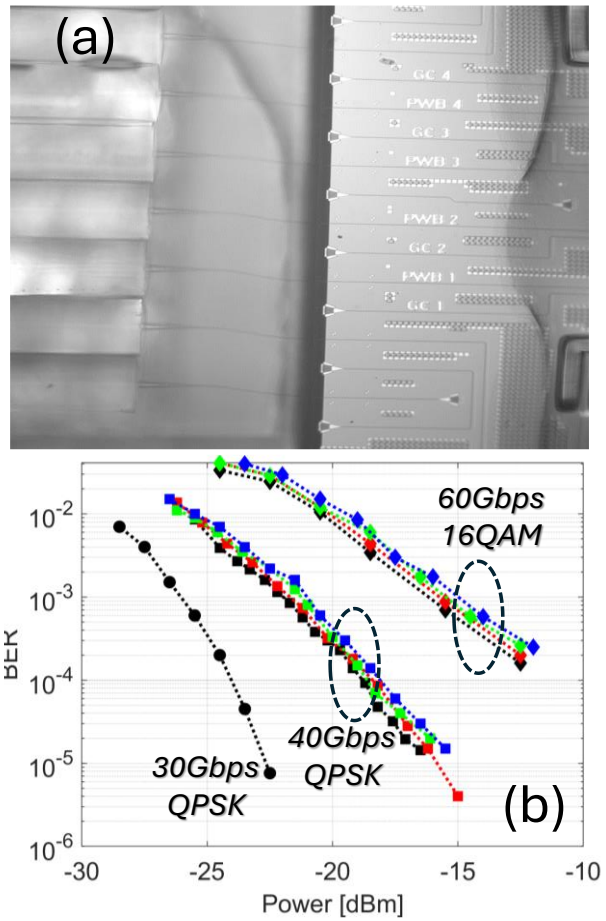

Figure 4 BER performance of the coherent optical receiver assembly, black: channel 1, red: ch. 2, green: ch. 3, blue: ch. 4 (a). Micrograph of the fiber to SOI interfacing realized through PWBs.

electrical pads on the top and bottom side, respectively. The assembly is shown in Figure 2. The green Rogers PCB is placed on a metal carrier, on top of a Peltier cell for thermal management. Flex cables are used to provide the DC controls while GPPO connections are used to collect the BPD outputs. The PCB is wedge-bonded to two Alumina PCBs acting as fan-out interposers, in turn wedge-bonded to the PIC. As a final packaging step, an 8-element FA has been connected to an edge coupler array through PWBs, on the north and south side, respectively. To be noted that the PIC orientation in Figure 2 is 90°-rotated with respect to its layout orientation in in Figure 1. Figure 4(a) shows the PWBs connecting each fiber of the FA to an edge coupler on the PIC. For each PWB, two fiber ribbons were glued manually in front of the PIC onto the assembly, one from each side. The distance between fiber and edge coupler is approx. 280µm, the lateral and vertical offset between fiber and chip is in the order of 10-20 µm. The offset between the facets can be compensated by the PWB trajectory. The PWB is fabricated using a commercial 3D lithography system that detects the fiber and the edge coupler, calculates from this data the optimal trajectory on the fly, and fabricates the corresponding PWB structure. Taper structures within the PWB adapt the mode field from the 10µm SMF fiber mode to the approximately 2µm mode field diameter of the silicon edge coupler. Finally, the PWBs are cladded with another commercial equipment, for both optical cladding as well as mechanical protection of the PWB. From a test loop from fiber (LO FA) to chip and directly back into a fiber (SIG FA), a loss per PWB of around 2.5dB was estimated. For testing the receiver assembly, a C-band continuous-wave laser has been externally modulated by an IQ Mach-Zehnder modulator driven by two channels of a 40 GHz and 100 GS/s digital-to-analog converter (DAC). the DAC was programmed to obtain QPSK and 16-QAM modulation formats at the rates reported in Figure 4(b). Each channel was tested individually (each color corresponds to a receiver channel) by varying the optical signal power through a variable optical attenuator. This way, the potential for 240Gbps transmission detection when employing all channels in a WDM fashion and 16QAM modulation format, and 160Gbps data rate in case of QPSK signals, was demonstrated. Both PCBs have been designed for supporting 50 GHz and that has been confirmed by the measured S parameters of each individual board. However, for modulation rates > 20Gbaud the digital signal processing at the receiver (mean squared error-based adaptive feed-forward equalizer) could not converge for QPSK format. We believe that the limited bandwidth of the assembly comes from the ~ 1 mm-long wedge bonds between the two PCBs, which could lead to parasitic inductive effects resulting in a growing impedance line mismatch with respect to RF frequency. Two long bonds also connect the SOI chip with the decoupling capacitors on the Alumina PCB (Figure 3), and both these two induced inductances have not been included in the preliminary simulation analysis of the whole system. Most probably, shorter bonds and gold rubber instead of gold wire would have prevented the issue. Such assumption was confirmed by comparing the measured optoelectronic (OE) bandwidth response of the four receivers, with an additional one obtained by directly probing one Alumina PCB RF output (after removing the wedge bonds) instead of the corresponding GPPO connection on the Rogers PCB (such comparison is not shown here). In the first case, each measurement revealed very pronounced power fluctuations typical of impedance mismatches and an envelope trend showing approximately 20 dB loss at 40 GHz, whereas the additional one attests a 9 dB loss at 40 GHz, confirming the detrimental impact of the long wedge bonds. The limited bandwidth of the whole receiver also justifies the high penalty between 30Gbps and 40Gbps QPSK (> 5 dB) deduced by Figure 4(b).

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