Integrated Reconfigurable Silicon Photonics Switch Matrix in IRIS Project: Technological Achievements and Experimental Results

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***Abstract*—This paper reports the performances of a silicon photonics optical switch matrix fabricated by using large-scale three-dimensional (3-D) integration. The wavelength selective optical switch consists of a photonic integrated circuit (PIC), with 1398 circuit elements, interconnected in a 3-D stack with its control electronic integrated circuit (EIC). Each PIC element can be trimmed or reconfigured by using metallic heaters. The EIC is designed to drive the heaters and to read the signal of monitor photodiodes integrated into the PIC. Small footprint and high energy efficiency are achieved in the PIC and the EIC. Automatic wavelength alignment of the optical circuits in the PIC to the ITU grid and fine temperature tuning of each photonic element to optimize the switch insertion losses are obtained by an optimization routine. A fully packaged switch with input/output fibers is tested both for optical and electrical characteristics as well as for the system performances. Fiber-to-fiber insertion losses of about 20 dB and channel isolation of −35 dB are achieved. Bit error rate characteristics at 25 Gb/s are evaluated. Perspective applications of the optical switch in optical transport and intra-data center networks are discussed.**

***Index Terms*—3-D photonic-electronic integration, colorless, directionless and contentionless (CDC) reconfigurable add and drop multiplexers (ROADM), integrated optical circuits, micro-ring resonator switch element, optical switches, photonic system-on-chip.**

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I. Introduction

THE technological advancements in silicon photonics transceivers for high-speed optical interconnects are boosting the research on new types of miniaturized optical switch devices with a capacity of many Terabit/s. Silicon photonics integration exploits the sophisticated and high performances manufacturing infrastructure and the materials used for CMOS electronic integrated circuits, and this enables the implementation of large scale integration, low cost and mass manufacturable optical switching devices.

In the European IRIS project (Integrated Reconfigurable silicon photonic based optical switch) [1] we designed, fabricated and experimentally evaluated a wavelength selective switch matrix with the architecture shown in Fig. 1. The concept of the IRIS optical switch was presented in [12] together with the design aspects, the specifications and simulation results. It has 4 network ports (NP1-NP4) and 8 local ports (LP1-LP8).

In one transmission direction, the sets of wavelength signals coming from the four network fibers are distributed to eight

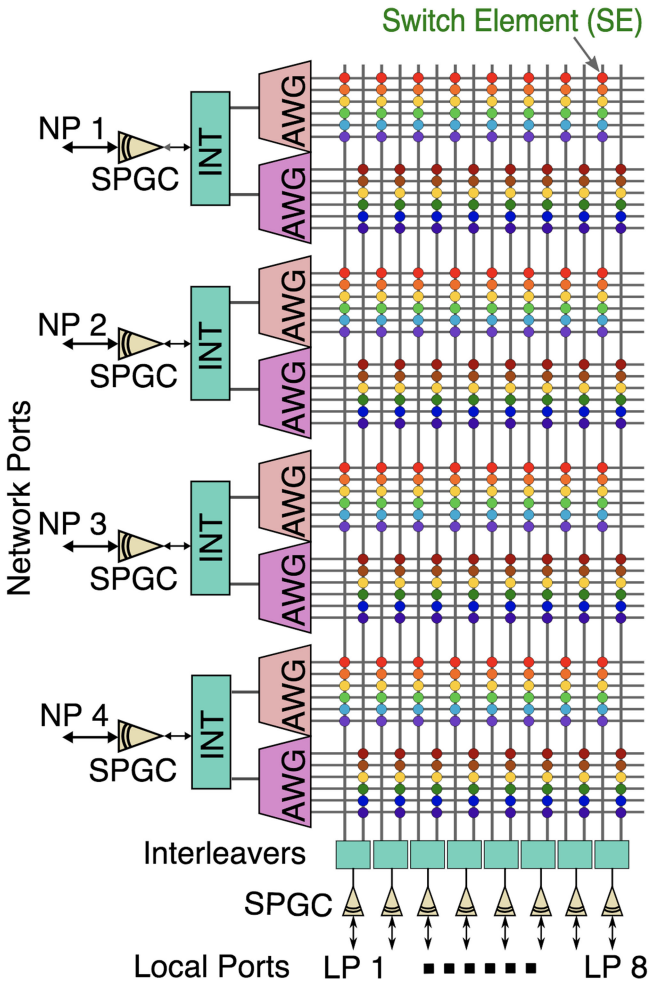

Fig. 1. IRIS switch architecture.

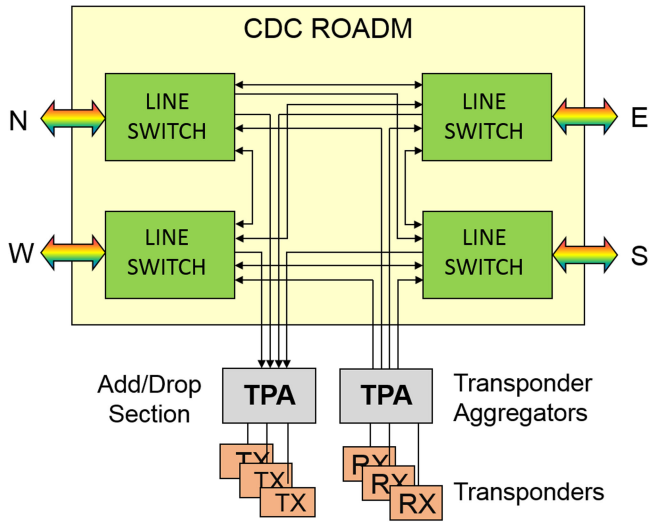

Fig. 2. Four-direction colorless-directionless-contentionless (CDC) ROADM.

local ports and in the opposite direction the wavelength signals generated in the eight local ports are injected into the network fibers.

The switch supports up to 12 wavelength division multiplexed (WDM) signals, 200 GHz spaced (in C-band) per each network port and includes different passive and active integrated circuits: single polarization grating couplers (SPGC) to couple light to/from optical fibers, a number of wavelength processing circuits like 12-channel interleavers (INT), 6-channel mux/demux based on array waveguide gratings (AWG), switch elements (SE) based on double micro-ring resonators (MRRs) and many monitoring photodiodes (PDs) at critical points in the circuits (not shown in the picture). Interleavers have been used to relax the isolation requirements of MRR and AWG, simplifying their design and fabrication. This increased the number of integrated elements (with 12 INT) and doubled the number of columns in the matrix from 8 to 16. The switch and differential path losses were kept low by designing low-loss interleavers and waveguide crossings.

The applications of such switch matrix can be envisaged in two areas: in metro optical transport networks and in future generation data centers. In optical transport networks, the trend is to enhance the current architectures of reconfigurable add and drop multiplexers (ROADM) with new colorless-directionless-contentionless (CDC) features [2]. This allows the operator to optimize resource utilization and support cost-effective re-routing functions in the event of faults. This implies extending the flexibility and automation to the ROADM end points and replace the fixed WDM mux/demux with a new optical switch named transponder aggregator device (TPA) [3]. An example of a four-direction CDC ROADM (direction north, south, west and east, named N, S, W and W respectively) is depicted in Fig. 2. The TPA is a switching sub-system used to distribute selected combs of wavelengths received from the 4 line switches to a set of receivers (RX) in the transponders and, in the opposite direction, the TPA is used to distribute the wavelengths from a set of transmitters (TX) in the transponders to 4 line switches. The switch matrix developed in IRIS project is suitable to perform TPA functions.

Optical switching has also been investigated for intra-data center networking of compute and storage resources thanks to the unique advantages of energy efficiency, low latency, cost reduction, wide bandwidth, and transparency to the bit rate and the protocol with respect to electronic switching [4]–[6]. The availability of low-cost, large scale integration, high port count optical switching matrices is the key aspect for the introduction of optical switching in data centers. A detailed overview of the silicon photonics switch matrices implemented so far has been reported in [7].

Wavelength division multiplexing has been proposed as interconnect technology for data center networking [8]–[11] to increase the link capacity of each single fiber connection. In [11] an optical circuit switch sub-system operates in combination with electrical packet switches and a possible implementation is shown in Fig. 3. The optical circuit switch (OCS) sub-system consists of 2 stages, namely a wavelength switch stage and a space switch stage. A key device for this architecture is the wavelength selective switch (WSS) used to aggregate and route the appropriate wavelengths received from the electrical packet switches (on top of the rack with a group of servers).

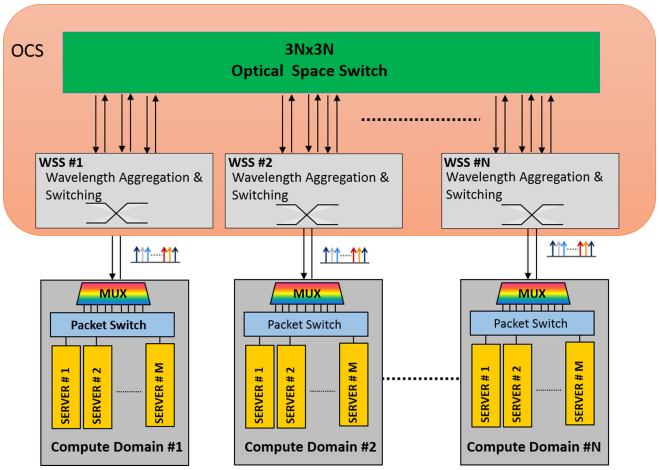

Fig. 3. Optical networking architecture in a data center.

The combs of aggregated wavelengths are then collectively routed toward the wanted destination by the optical space switch. The switch matrix developed in IRIS project can also be used as WSS device in the OCS, as presented in [27].

In this paper, we present the technological achievements and the experimental results of the integrated reconfigurable silicon photonics switch matrix. We fabricated a packaged device that comprises the fiber pigtailed photonic integrated circuit (PIC), its electronic integrated control circuit (EIC), and an external microcontroller. A key aspect in the packaging was the interconnection between the PIC chip and the EIC chip. Although monolithic integration of photonic and electronic circuits in the same chip is possible, the alternative solution based on a 3D integration of two separate chips was here preferred since it allows the use of a dedicated fabrication process for each chip and a more effective use of the chip area.

Our switch, like most of the integrated switching matrices prototypes demonstrated so far, due to the strong polarization sensitivity of silicon MRR, works with input signals having TE polarization. Although this allows to demonstrate most of the switch functionality with a minimum number of integrated elements, the switch industrialization will absolutely call for a polarization insensitive device because the optical fiber infrastructure in telecom and datacom networks is made by standard single-mode fibers. This can be achieved by implementing the switch with polarization diversity structure.

II. PIC Fabrication and Performance

The PIC was fabricated in the CEA LETI facilities on 8-inch Silicon-on-Insulator SOI wafers with 220 nm device layer and 2 μm buried oxide thicknesses. Deep-UV 193 nm optical lithography and reactive ion etching were used to define the waveguides. Ti/TiN heaters and epitaxial Ge photodiodes were fabricated to thermal tune the photonic devices and to on-chip monitor the optical signal. Fig. 4 shows an optical micrograph of a fabricated full PIC switching matrix.

The PIC includes many different types of functional components. As shown in Fig. 1, the optical switch requires grating couplers, interleavers, demultiplexers, tunable MRR switches, photodiodes, and other passive devices such as crossings and directional couplers. The design of these elements was presented in [12]–[16]. Multiplexers and demultiplexers were fabricated by using AWG. Table I shows the specifications of interleavers, AWGs and MRRs together with the measured performance. All three main functional components fulfill the specifications.

However, fulfilling the specifications of the individual building blocks is not sufficient for the correct functioning of the switch, which is composed of thousands of these and occupies a large chip space (65 mm^2). Therefore, fabrication must ensure the stability of component performances on the whole chip. Let

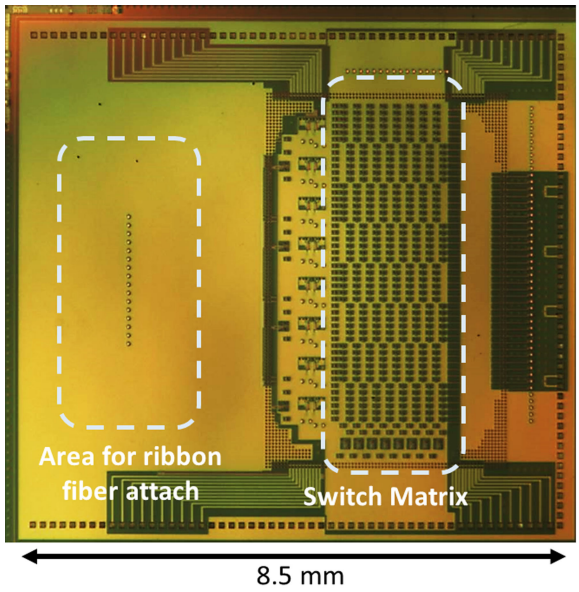

Fig. 4. Optical micrograph of the PIC. Note on the right the switch matrix and on the left the gratings for vertical in/out coupling of light from/to optical fibers.

TABLE I
Project Specifications and Measured Performance of Interleavers, Demultiplexers and Micro Ring Resonator Switches

Parameter	Specification	Measured
Interleaver loss	< 1.5 dB	**< 1 dB**
Interleaver bandwidth	>120 GHz	**>150 GHz**
Interleaver Isolation	> 20 dB	**> 20 dB**
AWG 1-dB bandwidth	>100 GHz	**>135 GHz**
AWG isolation @200GHz	> 10 dB	**>10 dB**
AWG isolation @400GHz	> 20 dB	**> 25 dB**
AWG loss	< 3 dB	**3-4.5 dB**
MRR 1-dB bandwidth	> 50 GHz	**> 70 GHz**
MRR isolation @200GHz	> 20 dB	**> 20 dB**
MRR isolation @400GHz	> 25 dB	**> 30 dB**
MRR isolation @600GHz	> 30 dB	**> 35 dB**
MRR isolation >1000GHz	> 35 dB	**> 40 dB**
MRR loss (*off* state)	< 0.1 dB	**<0.02 dB**
MRR loss (*on* state)	< 1 dB	**< 1 dB**
MRR tuning range	> 8nm	**> 12 nm**

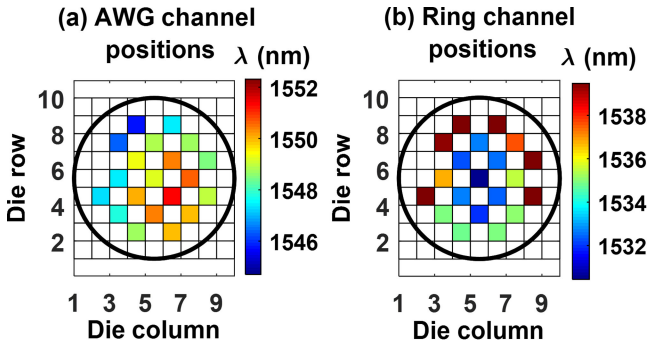

Fig. 5. Inter-die dispersion of channel positions of AWGs (a) and MRRs (b) along the wafer. Color code refers to the central AWG channel spectral position (left) and to the ring resonance (right).

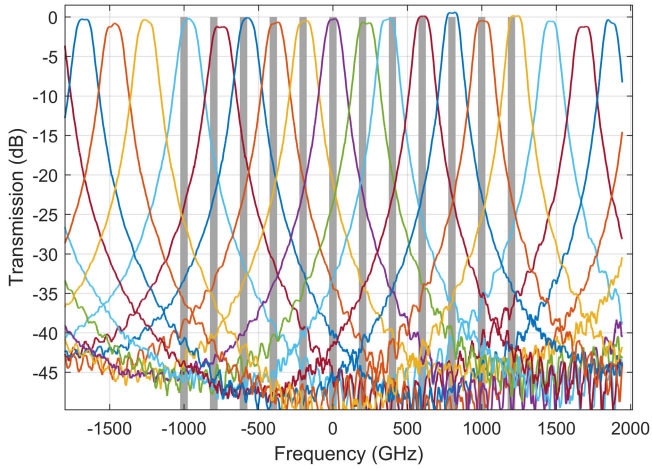

Fig. 6. Transmission spectra of all 12 drop channels (unheated). Grey bars are the nominal channel positions.

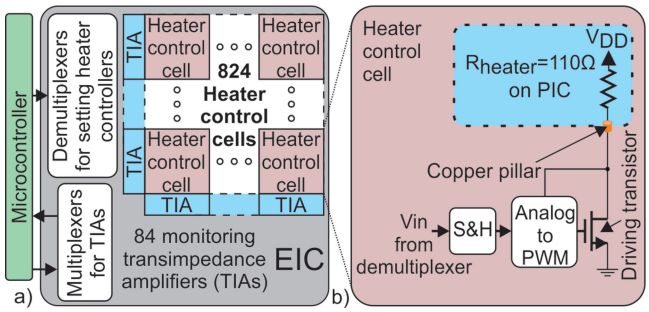

Fig. 7. Block diagram of the EIC (a) and a heater control cell (b).

us consider MRRs: the variability of their resonance position from die-to-die (inter-die) and within a die (intra-die) is crucial. The thermal trimming of the ring resonance can compensate the resonance fluctuations. The same applies to the interleaves. On the contrary, the large size of the AWGs renders difficult their tunability over a wide range by local thermal trimming. Our designs of tunable AWGs only allow tuning ranges of ∼200 GHz, whereupon the crosstalk increases excessively [14]. A solution is the thermal tuning of the whole PIC, which can allow shifting the AWG channels to the nearest ITU grid channel.

Fig. 5(a) shows the inter-die dispersion of the central AWG channel positions along the wafer. A variability higher than 5 nm is observed, which is related to the resolution and stability of the fabrication process. Better results could be expected by using 300 mm SOI wafers due to the more evolved silicon fabrication technology [17]. Alternatively, cascaded interleavers could be used to realize fully tunable demultiplexers [18]. Fig. 5(b) shows the wafer variability of the spectral position of the ring resonances, a variability of up to 9 nm is observed. The larger variation with respect to the AWGs is most likely due to the fact that the waveguides of the AWG were widened along the straight sections to reduce phase uncertainty [14], [19], while the MRR waveguides cannot be widened as they are very short and curved, resulting in higher-order modes being excited. However, for MRRs, the resonance variability is easier to deal with thanks to the thermal tuning offering wider tunability, and each MRR is individually addressable. The only potential issue is the position of the resonances in the *off* state since heating every MRR in *off* state would require too much power. Fig. 6 shows the intra-die variability of the ring resonances. More than a single free spectral range is shown. It is worth noting that the channels are aligned to their nominal positions within variations of ±75 GHz. When tuning these MRRs into the *on* state, their resonance position is aligned with the channel being switched.

Since each MRR is individually addressed, an issue can be raised about the thermal cross-talk between different MRRs. To study this effect, thermal simulations have been performed [12], [26]. We found that, when MRR are separated by 200 μm and 100μm, in the horizontal and vertical directions respectively, the thermal crosstalk is <0.5 °C. This results in a limited resonance wavelength shift of a few GHz. This prediction has been confirmed experimentally during our tests, as no thermal crosstalk from adjacent MRR has been detected.

III. EIC

The EIC was fabricated in STMicroelectronics' BCD8sp 0.16 μm technology from which only the CMOS part was used. Due to the large number of active photonic elements, the energy efficiency of the driver for controlling the heaters is of key importance. A high power consumption of the drivers would not only increase the total power consumption of the PIC+EIC sub-assembly but would also result in a considerable amount of heat dissipated from the EIC. Since the EIC is mounted directly on top of the PIC, this dissipated heat would locally change the temperature of parts of the PIC, consequently detuning the thermally tunable elements within the PIC.

As depicted in the block diagram in Fig. 7(a), the heater power is set by an external microcontroller. An integrated demultiplexer allows addressing all heater control cells. A multiplexer is used to output the voltages of the 84 monitoring transimpedance amplifier (TIA) cells. A block diagram of the heater control cell is depicted in Fig. 7(b). The actual heater value is stored in a sample&hold (S&H) element. An analog to PWM (pulse-width modulation) converter generates a PWM signal. The heater power, which is proportional to the duty cycle, is programmable by changing the value stored in the S&H element. The detailed circuit diagram is published in [20].

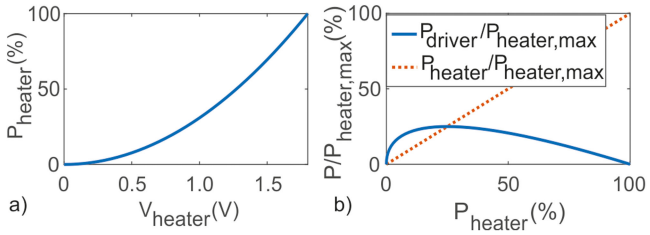

Fig. 8. Heater power P_{heater} versus the voltage V_{heater} across the heater resistor (a) and power dissipated by the driver and the heater depending on the heater power (b). Both for controlling the heater power with a constant voltage.

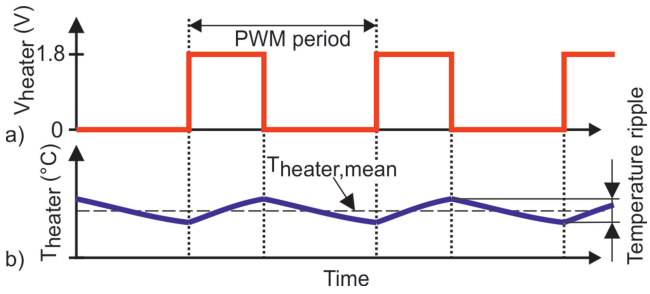

Fig. 9. Pulse width modulated voltage across the heater (a) and resulting thermal response of the heater (b).

In the EIC, the heater control cells, consisting of the PWM generation circuit and a driver, consume the main amount of power. The TIAs consume approximately 18 μW each, while the analog multiplexers (6 in total) consume approximately 0.55 μW each. The address decoders (4 in total) for addressing the heater control cells are consuming 14 μW each.

Using PWM for driving the heater resistor considerably improves the efficiency of the driving circuit, especially at low heating power. Using a constant voltage (analog) approach as shown in [12], the relation between heater voltage and heater power is quadratic as depicted in Fig. 8(a). Additionally, as shown in Fig. 8(b) for a low heating power, the dissipated power from the driver is considerably larger than the heating power.

Instead when using PWM, the mean heating power is defined by the duty cycle (i.e., the ratio of the "*on*"-time over the whole period) of the PWM signal. When operated with a PWM signal, the driving transistor is either *on* or *off*. Consequently, the big advantage is that the power consumption of the driving transistor is always close to zero. The mean power consumption of the heater resistor can be tuned from zero to V_{DD}^2/R_{heater}, where V_{DD} is the heater supply voltage and R_{heater} is the heater resistance, by changing the duty cycle. However, during the "*on*"-time of the PWM signal the temperature of the heater will increase, while it will decrease during the "*off*"-time as depicted in Fig. 9.

This temperature ripple can periodically detune the photonic elements. The shorter the PWM period, the smaller this temperature ripple gets. For the present device, with a thermal time constant of $\sim$4 μs, a PWM frequency of $\sim$7.58 MHz is required in order to guarantee a thermal ripple below the critical limit. Using a fully digital circuit, for a 7bit PWM control, implies a clock frequency around 1 GHz to generate the PWM signal.

In the used technology we achieved clock frequencies up to 1.2 GHz for the PWM generation circuit, for a smaller test circuit [21]. Using the analog to PWM converter circuit allows achieving much higher PWM frequencies, especially for duty cycles close to 50%, which cause the largest thermal ripples. Our analog-digital (hybrid) PWM approach reaches PWM frequencies in the range of 70 MHz [20], which is almost ten times larger than for the fully digital PWM approach. For a realistic heating scenario (16 MRRs are *on*, the remaining MRRs are tuned by an average heater power of 1.5 mW for compensating process tolerances), the power consumption of the hybrid approach is approximately 94% lower compared to the constant voltage (analog) heater control [21]. A limiting factor of the analog and the hybrid approach is the storage of the heater power data within an S&H element. The inevitable leakage of the S&H elements necessitates periodic refreshes.

Nevertheless, we proved that it is possible to control a PIC with a large number of heaters using a very power efficient analog-digital approach (Fig. 7(b)). The power dissipation of the 768 heater control cells for the 48 $\times$ 16 switches is found to be approximately 175 mW. This approach can be scaled up to even a larger number of controlled elements using smaller (and therefore faster) technology nodes for the EIC where the fully digital PWM approach becomes competitive. In fact, with a smaller feature-size technology it is easier to reach the required PWM frequency and the fully digital PWM control approach does not need any refreshes since the heater power is stored in a digital register.

IV. Packaging

The very large scale integration level of the switch matrix requires a stacked 3D co-integration of the PIC and of the EIC which leads to more than 2000 electrical interconnects between the two different chips. A 50 μm pitch copper pillar technology was selected. Additionally, the PIC must also be interfaced with more than 10 fibers [22], [23]. In order to use micro-pillar arrays, the electronic wafer was post-processed using electroplating semi-additive process of a Ti/Ni/Cu metallic stack through a thick resist mask. An additional layer of eutectic solder (e.g., SnAg) was deposited on the top of the micro pillar. The photonic wafer was processed with under-bump metallization (UBM) pads defined by a Cu/Ni/Au stack. Then, the chips were defined and PIC/EIC interconnections were achieved by flip-chip bonding. The result for a single interconnection is depicted in Fig. 10. Less than 1 Ω serial resistance by contact was measured. Even though a pitch of 50 μm was used, this integration technology is scalable in terms of interconnection density with a current minimal pitch of 30 μm. Finally, the PIC average temperature needs to be stabilized to avoid wavelength shift of the optical elements in the PIC caused by the operation of the EIC and ambient temperature variation.

Fig. 11 shows the fully packaged device on the module board, which contains the PIC+EIC sub-assembly, optical connector, Peltier thermo-electric cooler (TEC), module and host board.

The module board (Fig. 11(c)) supports the TEC and the PIC+EIC sub-assembly and provides the thermal connection between TEC and the package. A metal sheet is glued to the hole of the module board using epoxy casting resin. Then, by

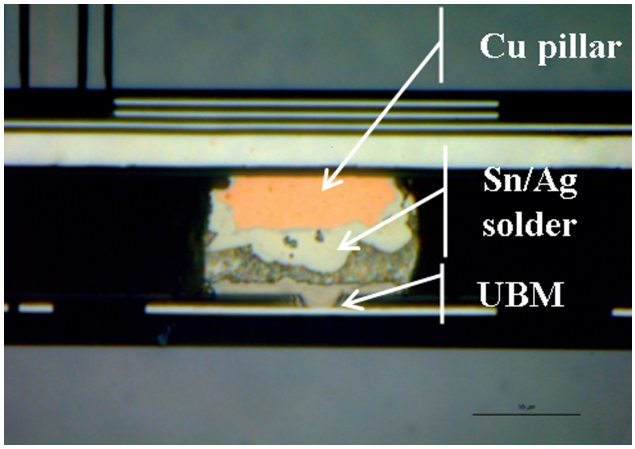

Fig. 10. Cross section of PIC (top) and EIC (bottom) dies with UBM stack and micro pillars.

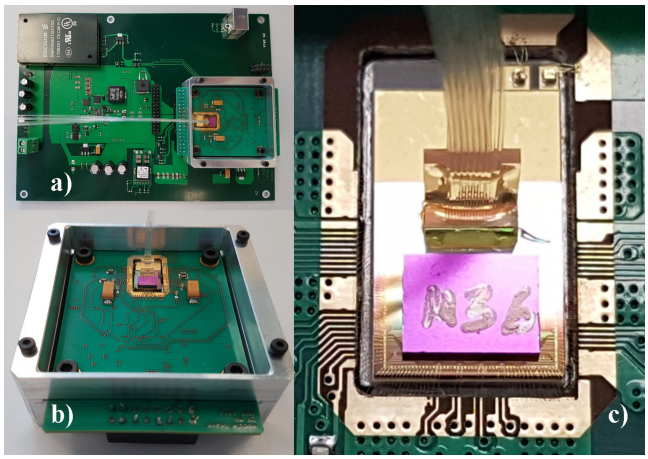

Fig. 11. (a) Whole assembly on host board; (b) Module board inside the Aluminum package; (c) Detailed view of the TEC and the 3D PIC-EIC sub-assembly wire bonded to the module board and pigtailed with a fiber array.

means of a die attach machine (Finetech model pico Ma), TEC and PIC+EIC sub-assembly are placed on top of the metal sheet using a silver-filled epoxy. At that point, electrical connections are realized using 25 μm diameter gold wires, via ball-wedge wire bonding technology with a TPT HB16 bench wire bonder. A total of 138 connections are realized. Subsequently, a V-groove assembled 16-fiber array is vertically coupled to the grating couplers. The fibers in the array are standard single mode fibers. The coupling and pigtailing of the fiber array to the chip has been achieved by an active alignment process using an automatic alignment bench. The bench is composed by 6 axes micromanipulators. The fiber array position is optimized employing an automatic peak picking procedure (excess losses = 0.5 dB).

The pigtailing has been done by a UV curable resin, used as optical index-matching as well, resulting in coupling losses below 4 dB/grating.

In order to be more versatile, a removable packaging solution was conceived where the module board is interfaced with a host board (Fig. 11(a)). The aluminum-housing package offers a robust solution in terms of protection of the components and optimal thermal dissipation.

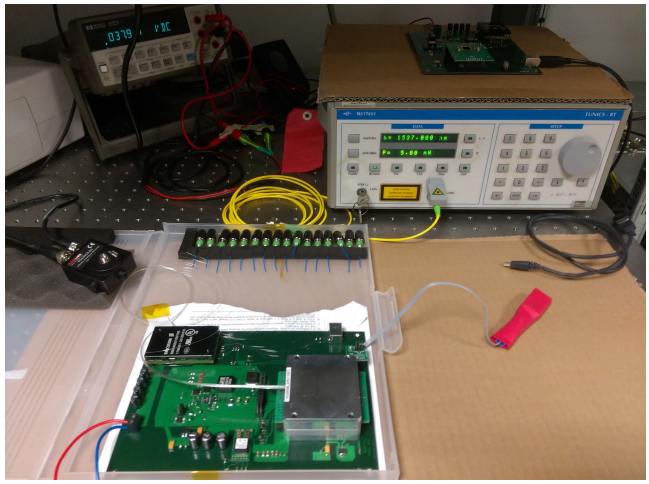

Fig. 12. Packaged device in the device configuration test set-up.

Fig. 12 shows the fully packaged device in the test set-up. The packaging has been carried out by Technische Universität Wien and the Universitat Politècnica de València.

Note the red connector on the right which allows interfacing the board to a PC via a USB connector, the two red-blue wires on the bottom left for the power supply of the board and the set of fiber connectors on the top. The configuration tests of the switch, reported in chapter VI, were performed using a tunable laser (top right) and an InGaAs photodetector (middle left).

V. Calibration

The three main building blocks of the PIC, namely the AWG, the interleaver and the double MRR switch element, must be thermally tuned to align their spectral response to the specifications. The calibration procedure allows determining the optimal working condition for each component, i.e., the voltages/currents needed to trim its characteristics to the desired value. All the information collected during the calibration are stored in a look-up-table (LUT) that can be used to set up the wanted switching configuration or to restore the default position of the PIC elements. We aligned the spectral response of AWGs, interleavers and MRR switch elements following three different methods, specific to each component.

The robustness of the AWG design against fabrication errors makes the 8 MUX blocks on the PIC very similar to each other in terms of spectral response. For this reason, we align all the AWGs at once to the ITU grid by means of the Peltier cooler. Still, dedicated heaters placed on top of the AWG could be used for fine spectral tuning [14].

After AWG alignment, the interleavers are aligned to the AWG channels through a stochastic algorithm based on the Globalized Bounded Nedler-Mead (GBNM) method [24], [25]. The target function that the algorithm aims to maximize is the optical power transferred into one arm of the interleaver. As shown in Fig. 13(a), an optical signal was injected into the input waveguide of the interleaver. The signal frequency was repeatedly swept at high speed over a range of 100 GHz (AWG 1-dB bandwidth) centered to one frequency of the ITU grid. The frequency swept signal is collected and integrated by a slow Ge

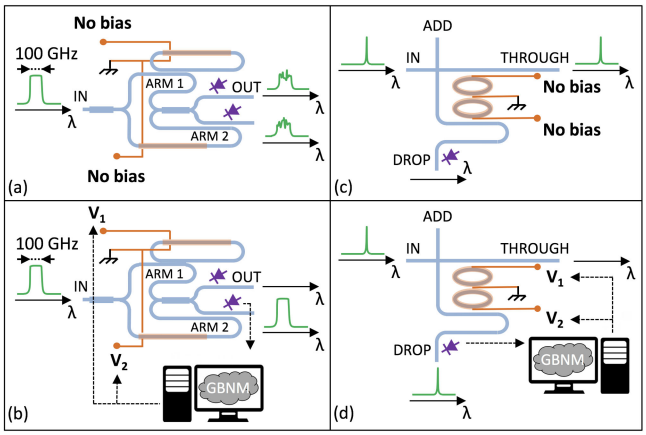

Fig. 13. Schematics of the automatic optimization of the interleaver (left panels) and of the MRR switch node (right panels).

photodiode placed at the output port of the interleaver. The optical power detected by the photodiode depends on two bias values (V_1 and V_2) applied to the heaters placed over the interleaver arms (first stage of the device presented in [18]). The optimal configuration is the one that maximizes the power coupled into the photodiode (see Fig. 13(b)). Thus, by feeding the photodiode read-out into the GBNM algorithm, we can automatically find (after a few steps) the optimal V_1 and V_2 bias values aligning the interleaver to the chosen ITU frequency.

Once the interleavers are aligned to the ITU grid and their transmission is optimized, we applied the GBNM algorithm to the MRR switch elements. In this case, Fig. 13(c), the tunable laser was set at the ITU frequency that must pass through the node in the *on*-state. The target function in the optimization is the optical power collected by the photodiode at the switch element drop port. The GBNM algorithm finds the best two bias values to be applied to the MRR heaters to drive the node in *on*-state (see Fig. 13(d)).

We implemented the GBNM routine in an NI LabView interface, which employed a Tunics BT as laser source and the Ge photodiodes on the PIC as feedback monitors. The program set the different bias on the EIC as well following the optimization algorithm instructions. To calibrate the switch and generate a LUT for all the different photonic components (AWGs, 12 interleavers, 384 switch nodes) it took about 12 hours. This process can be significantly shortened by increasing the communication speed between the chip host board and the computer (currently @ 9600 bps).

In the end, the LUT table contains the values of bias (Vi) to be applied to each heater in the PIC in order to align the element to the ITU grid and optimize the transmission of the component, resulting in total a matrix of 793 values.

VI. Device Configuration Test

After generating the LUT, we moved to test the device performances with CW optical signals as inputs. A test result is shown in Fig. 14 where the PIC was used in the add configuration through the red and blue paths (Fig. 14(a)). A 6 dBm optical signal was injected into the input fiber and the output

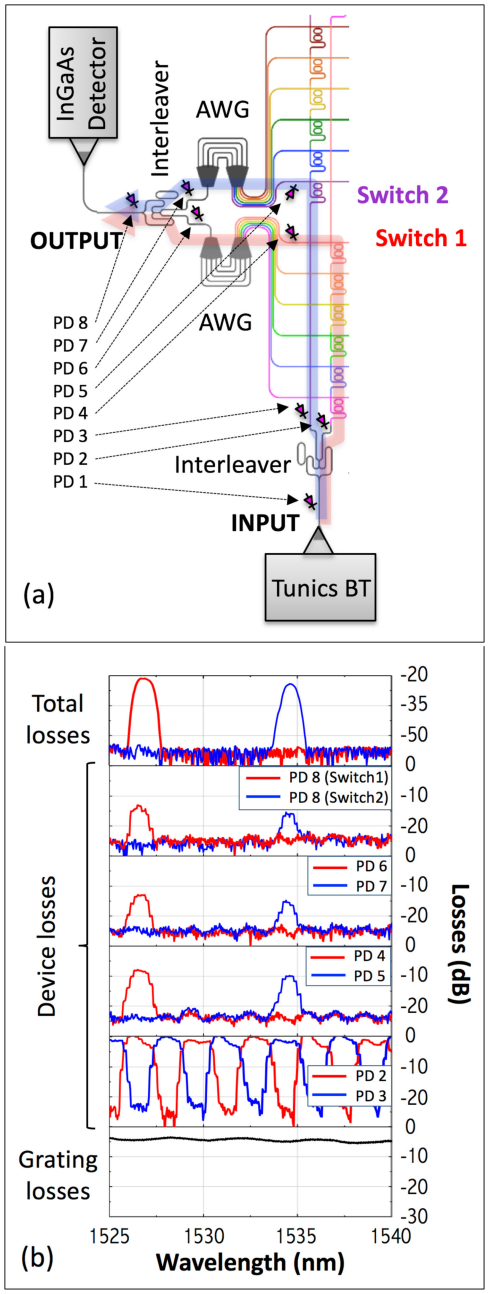

Fig. 14. Optical paths of the switch matrix set in the add configuration (a), with measured performances acquired at the different stages in- and off-chip (b).

signal was measured by an InGaAs photodetector coupled to the output fiber. Fig. 14 (b, top panel) shows the fiber-to-fiber insertion losses for two different settings of the switch matrix. Red path when the switch 1 is in the *on*-state (we add to the line the 1526,5 nm channel), blue path when the switch 2 is in the *on*-state (we add to the line the 1534,3 nm channel). The spectrum represents the transmitted signal at the output fiber, with respect to the signal at the input fiber. The channel insertion loss is about 20 dB with a channel isolation better than 35 dB.

To determine the different contributions to the insertion losses we tracked the signal propagating in the chip thanks to the on-chip monitoring PDs. In fact, the transmission spectra in Fig. 14(b) refer to those signals that were measured by various

monitor photodiodes as indicated in Fig. 14(a). The bottom panel represents the transmission loss due to the coupling of the optical signal from the input fiber to the PIC (about 4 dB). The four central panels represent the on-chip additional losses, referred to the signal level detected by the first photodiode (PD 1).

Note that:

- The second panel from the bottom shows the interleaver transmission where the routing of the input signal to one or the other switch matrix column can be observed accordingly to the separation of the channels into even (red path) and odd (blue path) wavelengths (almost 0 dB device losses on the routed channels and more than 25 dB channel isolation). It is important to point out that the PDs have a limited dynamic range of 25 dB.
- The third panel reports the spectrum when switch elements are thermally tuned (switch 1 red path and switch 2 blue path measured by PD 4 and PD 5, respectively). Note the free spectral range of 19 nm and the loss of about 10 dB, which includes interleaver, MRRs (one in the *on*-state and the others in the *off*-state), crossings, and waveguides. The loss value is larger than expected due to non-optimal waveguide crossings having a wavelength-shifted response [26].
- The fourth panel shows the signal after the AWG (less than 4 dB of additional losses). Here we note the optimum alignment of all the components to the AWG channels.
- The fifth panel is the signal at the output of the last interleaver (PD 8) confirming the low interleaver losses.

This analysis shows that the total channel losses of 22 dB can be decomposed into 8 dB of grating couplers losses and 14 dB of on-chip losses. Of the latter, the largest contribution is due to the signal propagation along the matrix as confirmed by this full chip test from which the isolated component losses can be inferred as reported in Table I (interleaver loss of <1 dB, AWG loss of 4 dB, MRR switch loss of 1 dB).

Preliminary statistics performed on two identical packaged switches evidence that the differential path loss between the shortest and the longest optical paths in the switch matrix is about 6 dB. This analysis shows also that less than 3% of all optical and electrical components are not working properly due to production inaccuracies.

VII. Transmission Performances Tests

In this section, we report the transmission performance tests of the switch used as a TPA with a 25 Gbps optical signal. In order to experimentally evaluate the most critical performances of the switch, two tests were performed:

1. the single channel transmission test
2. the interferometric crosstalk test

This last test addresses the most relevant issue in the TPA performance as described in [12] where, in the worst-case scenario, up to three interferers at the same wavelength of the channel (signal) under test (co-channel interferers) are present.

A. Single Channel Transmission Test

The aim of this test is to evaluate the transmission performances of the switch when only the channel under test is present in the system. The set-up used for this test is shown in Fig. 15.

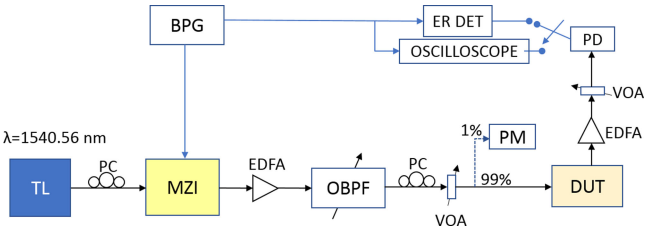

Fig. 15. Test set-up for the single channel transmission test.

A tunable laser light set at 1540.56 nm is modulated at 25 Gbps by a $LiNbO_3$ Mach-Zehnder interferometric (MZI) intensity modulator with a pseudo random binary sequence (PRBS) data pattern having a length of $2^{31}-1$ bits. Care is taken to send to the MZI modulator a carrier with the right polarization state which is manually adjusted through a polarization controller (PC). The optical modulated signal is amplified by an erbium doped fiber amplifier (EDFA) set at $+18$ dBm of output power and the signals plus the ASE noise is filtered by a tunable optical band-pass filter (OBPF) with a bandwidth of 100 GHz.

The modulated signal is transmitted through a single mode fiber to the switch input and the input power level is controlled by a variable optical attenuator (VOA). In addition, the input polarization is adjusted to match the TE input polarization used in the switch thanks to the high-speed photodetector (PD) after the input grating monitoring the coupled power. The signal is sent at the input port NP1 (see Fig. 16) and it enters the switch matrix at the row $\lambda 7$ after it has been transmitted by an interleaver and an AWG de-multiplexer. In the matrix, the switch element identified by the red spot in Fig. 16, i.e., the one in the fourth row and first column, is activated to drop the signal to the LP1 port. The output signal is then amplified by an EDFA acting as pre-amplifier, with the output power set at $+13$ dBm, to compensate for the switch internal loss. The signal is then filtered by a bandpass filter with a 100 GHz bandwidth (to attenuate the ASE noise of the EDFA) and a VOA just before PD is used to vary the received power level for the BER curves acquisition. The signal is either sent to a BER tester or to an oscilloscope to observe the eye diagram.

The switch input power level was $+1.5$ dBm and the output power level was -21 dBm summing to a total loss of about 22.5 dB, in line with the losses reported in the previous section.

The BER curves are shown in Fig. 17. The dashed line with crosses represents the result of the back to back transmission which sets the performance of the set-up while the dotted red line with squares represents the result of the single channel transmission: the power penalty is about 1 dB. The BER is measured until -9 dBm condition at which the BER tester saturates and does not allow to get larger BER. The power penalty is due to a small degradation of the optical signal to noise ratio (OSNR) in the single channel test (21.8 dB) respect to back-to-back test (23.42 dB).

B. Interferometric Crosstalk Test

The crosstalk is a system effect coming from the finite isolation of the various elements cascaded in the switch: MRR, INT, AWG and waveguide crossings. Two types of optical crosstalk

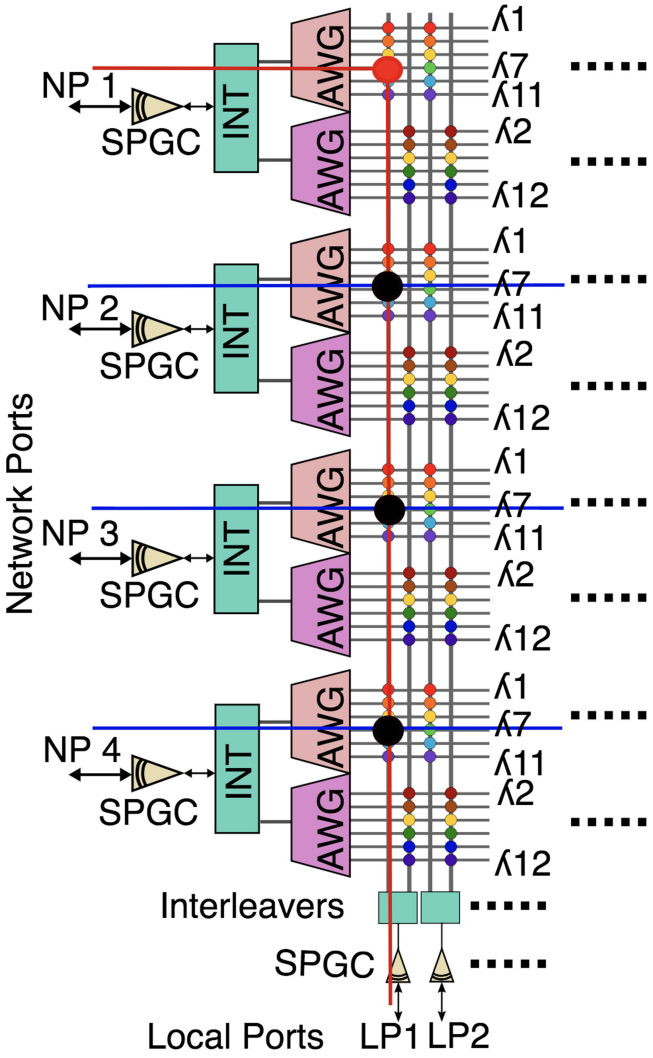

Fig. 16. Optical paths of signals used in transmission tests. Red spots indicate the MRR set to *on* and the black spots indicate MRRs set to *off*. The other MRRs were left uncalibrated. Red lines indicate the path of the channel under test, blue lines indicate interferometric interferes paths.

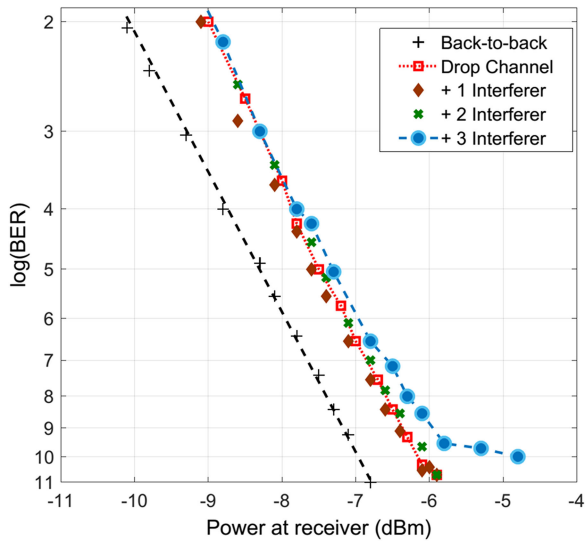

Fig. 17. BER curves: Back to back, single channel and with interferometric crosstalk.

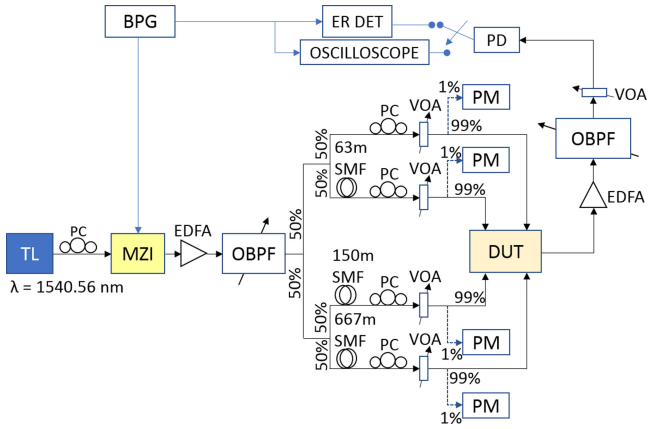

Fig. 18. Test set-up used for interferometric crosstalk test.

are present in our switch matrix: interferometric crosstalk, arising from disturbing channels at the same wavelength of the channel under test and inter-channel crosstalk, arising from disturbing channels at wavelengths different from that of the channel under test. In this paper we experimentally investigated the interferometric crosstalk since it is the most detrimental one [12].

For the interferometric crosstalk test, we used the set-up as for the single channel transmission test and we added three interferometric interferers as shown in Fig. 18. The 25 Gbps modulated signal is split into four optical data streams, the first of which acts as the channel under test and is sent to the λ7 row of the matrix via the NP_1 input and is dropped at the LP1 output port (see Fig. 16). The other three optical signals, after appropriate decorrelation through fiber spools of 63m, 150 m, and 667 m, constitute the interferometric interferers at the same wavelength of the channel under test. These interferers are sent at the line input ports NP_2, NP_3 and NP_4, they are demultiplexed by the INT and AWG blocks and enter the switch matrix at the λ7 rows.

The polarization is carefully controlled at each of the four-line input ports NP_1, NP_2, NP_3, and NP_4. VOAs, 1% optical power taps and power monitors (PM) are also used to read and equalize at +1.5 dBm the power level of the channel under test and those of the three interferometric interferers at the switch input.

The channel under test is dropped at the LP1 port (see Fig. 16) by activating the switch element in the fourth row and first column of the matrix, indicated by a red spot in Fig. 16, while the switch elements indicated in black corresponding to the matrix rows λ7 of the other sub-matrix structures are set in off. The dropped signal plus the interferometric crosstalk is then amplified by an EDFA, with the output power set at +13 dBm. Finally, the signal is filtered by an OBPF having a 100 GHz bandwidth (to attenuate the ASE noise) and a VOA just before the PD is used to vary the received power level for the BER curves acquisition. The power level of the dropped signal at the switch output was −21 dBm.

BER curves are shown in Fig. 17. The BER curves of the channel under test (injected at NP_1 port) plus the first and second interferers, inserted at NP_2 and NP_3 ports respectively, are

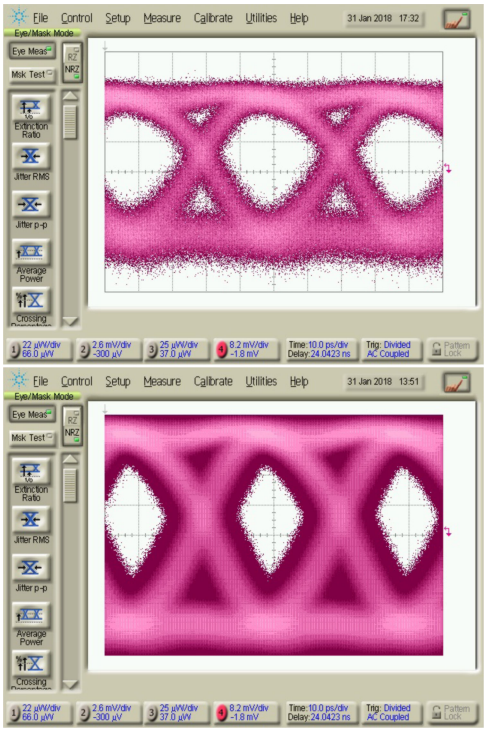

Fig. 19. (Top) Eye diagram of the signal dropped through IRIS switch with single channel test. (Bottom) Eye diagram of the signal dropped through IRIS switch with channel under test plus the interferers (acquisition time >2 hours).

shown. There is no power penalty with respect to the single channel transmission BER curve. When the third interferer is also added at port NP_4 a small power penalty of less than 0.5 dB is measured together with a BER floor around 10^{-10}. This is due to the differential path loss between the channel under test, having the longest path inside the matrix, and the third interferer, which has the shortest path. This differential path loss in favor of the interferer was 6 dB plus 1 dB since the interferers do not undergo, like the channel under test, the loss of an activated MRR, leading to an additional power difference between the channel under test and the third interferer of 7 dB. This causes an increase of the interferer power that eventually causes the BER floor. A similar BER floor was found with only one interferer injected at NP_4 port confirming the detrimental effect of the differential loss on crosstalk performance.

Eye diagram recorded during these tests are reported in Fig. 19(top) for the single channel test and in Fig. 19(bottom) for the interferometric crosstalk test with three interferers. The acquisition time was more than 2 hours and the tests showed eye opening.

VIII. Conclusions

The integration scale of our switch is one of the largest ever realized with 1398 photonic components in a 65 mm^2 chip area. To the electronic control of such a large-scale integration chip, a 3D integration of PIC with EIC was implemented which yields one of the highest chip to chip interconnect density ever reported for integrated optical devices for Telecom and Datacom applications. Based on a solid design, the PIC has characteristics compliant with the requirement specifications for the spectral response, while the losses are larger than expected. We believe that this is caused by the finite resolution of the fabrication process and by the thickness variation in the 200 mm SOI wafer, as witnessed by the significant wavelength channel shift of up to 10 nm with respect to the design values in the wavelength selective integrated circuits. Compensation of these on-wafer variations is possible in the MRRs and the interleavers due to their small size. On the contrary, this is very challenging in large components like the AWG and it is not possible in purely passive structures like the grating couplers and the waveguide crossings. Indeed, large propagation losses on the columns and rows of the optical switch matrix were measured. Therefore, a 60 nm lithographic node and the 300 mm wafer technology should be considered to improve the resolution and the stability of the fabrication process. In this way, the wavelength selective massive integrated circuits could benefit from the improved characteristics of the passive components and, in turn, from a dramatic reduction of the insertion losses.

The EIC was one of the key enablers in our device implementation due to the large number of optical components in the PIC. EIC/PIC integration allows the independent control of each one of them with a tight power constraint, a high accuracy, and a small footprint. In addition, it permits the automatic calibration and the build-up of the LUT by using the monitoring photodiodes. Despite the high quality of the reported results, many improvements to our switch device are still needed to turn it into a commercial product. The possible improvements that could be implemented are: providing polarization independence by using a polarization diversity scheme, reducing loss by using a better fabrication process and by integrating semiconductor optical amplifiers (SOA) blocks, reducing the differential loss to improve the crosstalk performance and finally increasing capacity by increasing the number of input/output ports and by increasing the number of wavelength channels in each network line.

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Authors' biographies not available at the time of publication.