Optical Transmitter Based on a 1.3-μm VCSEL and a SiGe Driver Circuit for Short-Reach Applications and Beyond

Antonio Malacarne, Christian Neumeyr, Wouter Soenen, Fabio Falconi, Claudio Porzi, Timo Aalto, Jürgen Rosskopf, Johan Bauwelinck, and Antonella Bogoni

***Abstract*—Long-wavelength vertical-cavity surface-emitting lasers (LW-VCSELs) with emission wavelength in the 1.3-μm region for intensity modulation (IM)/direct detection optical transmissions enable longer fiber reach compared to C-band VCSELs, thanks to the extremely low chromatic dispersion impact at that wavelength. A lot of effort has been recently dedicated to novel cavity designs in order to enhance LW-VCSELs' modulation bandwidth to allow higher data rates. Another approach to further improve VCSEL-based IM speed consists of making use of dedicated driver circuits implementing feedforward equalization (FFE). In this paper, we present a transmitter assembly incorporating a four-channel 0.13-μm SiGe driver circuit wire-bonded to a novel dual 1.3-μm VCSEL array. The short-cavity indium phosphide buried tunnel junction VCSEL design minimizes both the photon lifetime and the device parasitic currents. The integrated driver circuit requires 2.5-V supply voltage only due to the implementation of a pseudobalanced regulator; it includes a two-tap asymmetric FFE, where magnitude, sign, relative delay, and pulse width distortion of the taps can be modified. Through the proposed transmitter, standard single-mode fiber reach of 20 and 4.5 km, respectively, for 28- and 40-Gb/s data rate has been demonstrated with state-of-the-art power consumption. Transmitter performance has been analyzed through pseudorandom bit sequences of both 2^7-1 and $2^{31}-1$ length, and the additional benefit due to the use of the driver circuit has been discussed in detail. A final comparison with state-of-the-art VCSEL drivers is also includedt.**

***Index Terms*—Access networks, BiCMOS integrated circuits, optical fiber, optical intensity modulation, optical interconnections, vertical cavity surface emitting lasers.**

Manuscript received October 24, 2017; accepted November 29, 2017. Date of publication December 13, 2017; date of current version February 27, 2018. This work was supported by the European projects FP7 RAPIDO under Grant 619806, H2020 ROAM under Grant 645361, and FP7 PHOXTROT under Grant 318240. *(Corresponding author: Antonio Malacarne.)*

A. Malacarne, C. Porzi, and A. Bogoni are with the Institute of Communication, Information and Perception Technologies, Scuola Superiore Sant'Anna, 56124 Pisa, Italy (e-mail: antonio.malacarne@santannapisa.it; claudio.porzi@sssup.it; antonella.bogoni@sssup.it).

C. Neumeyr and J. Rosskopf are with Vertilas GmbH, 85748 Garching, Germany (e-mail: neumeyr@vertilas.com; rosskopf@vertilas.com).

W. Soenen and J. Bauwelinck are with imec, IDLab, Department of Information Technology, Ghent University, 9000 Ghent, Belgium (e-mail: wouter.soenen@ugent.be; johan.bauwelinck@ugent.be).

F. Falconi is with the Photonic Networks and Technologies National Laboratory, National Interuniversity Consortium for Telecommunications, 56124 Pisa, Italy (e-mail: fabio.falconi@cnit.it).

T. Aalto is with the VTT Technical Research Centre of Finland, FI-02044 Espoo, Finland (e-mail: timo.aalto@vtt.fi).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JLT.2017.2782882

I. Introduction

LONG-WAVELENGTH vertical-cavity surface emitting lasers (LW-VCSELs) keep attracting more and more attention due to the many advantages associated to their use, i.e., potential low cost due to the very cost competitive production method, low power consumption, robustness to high temperatures, potential for hybrid integration on Si-based transceivers and single-mode operation [1], [2]. For all these reasons, edge emitting distributed feedback (DFB) lasers as well as electro-absorption modulated lasers (EML), which represent the choice for today's single-mode short-reach solutions, are expected to be replaced by LW-VCSELs in the near future. Up to now, single-mode LW-VCSELs have been developed based on GaInNAs and InP material. However, only InP-based VCSELs can cover wavelengths for the full O-band (1.3 μm range), C- and L-band. Recent research for optical interconnects mainly focused on 1.55 μm VCSEL links achieving data rates up to 56 Gb/s [3], [4]. However, positive chromatic dispersion (CD) of standard single-mode fiber (SSMF) in the C-band combined with the positive frequency chirp induced by direct modulation of the cavity laser, limits the transmission distance to less than 1 km at 40 Gb/s and 500 m at 50 Gb/s [3]–[6], therefore not matching the fiber reach requirement for large data centers (2 km) [7]. The use of the 1.3 μm regime would extend the fiber reach due to the low chromatic dispersion, therefore making their use suitable for building-to-building applications, inter-data center scenarios and up to the access segment. Error-free operation through a 25 Gb/s directly modulated 1310 nm-VCSEL based on GaAs wafer fusion technology, was recently demonstrated up to 10 km of SSMF, with data rate limited by the 3 dB-modulation bandwidth (11.5 GHz) [8]. Through a short-cavity design a InP-based VCSEL with modulation bandwidth of 15 GHz and emission wavelength of 1275 nm was demonstrated over 25 km of SSMF at a bit rate of 25 Gb/s [9]. In that case such a result was also possible thanks to the chromatic dispersion that, at that wavelength, is negative therefore leading to optical pulse narrowing.

To enhance the modulation speed, a lot of effort has been recently devoted to both develop novel VCSEL designs and dedicated driver circuits implementing feed forward equalization (FFE), sometimes combined with multi-level modulation formats [3], [5], [10]–[22]. Concerning the VCSEL design, Vertilas has already demonstrated, through its InP platform, 1.55 μm-VCSELs with a bandwidth up to 18 GHz and an optical power up to 4 mW at room temperature [3], [6], and the 1.3 μm solution presented in this manuscript achieves similar performance. Concerning the use of proper drivers, the majority of the proposed transmitters including driving circuits, drives the anode of the VCSEL to minimize the supply voltage for both the output and biasing stage [10]–[16]. Nevertheless, in all cases the driver circuit still operates at a lower supply voltage than the VCSEL or output stage. Furthermore, higher data rates can be achieved if the cathode is driven instead of the anode because the slower p-type transistors are avoided at the output node [17]–[22]. Data rates up to 71 Gb/s have been achieved for cathode driven 850 nm-VCSEL [21] whereas 56 Gb/s is the fastest bit rate obtained in case of 1.5 μm VCSELs [3], [22]. Unfortunately, VCSEL supply voltages from 3.1 V up to 5.8 V are associated to these results. Hence, there is a strong need to limit the supply voltage discrepancy between driver and cathode-driven VCSELs so as to reduce the power consumption and simplify the supply voltage interfacing provided by vendors. Ultimately, a single supply operated VCSEL driver or even VCSEL link is pursued as already reported in [5].

Here we present a transmitter assembly that embeds a novel high-speed 1325 nm-VCSEL wire bonded to the low-power SiGe driver circuit including 2-tap FFE from [5], targeting 28 Gb/s and 40 Gb/s over an unprecedented SSMF length. The manuscript represents an extension of [23].

Section II describes the VCSEL structure realized by Vertilas and reports on its static and dynamic characterization including modulation bandwidth and transmission tests at a bit rate of 28 Gb/s. Section III describes the driver circuit including performance characterization and explanation of the operation of the included pseudo-balanced regulator. In Section IV the transmitter assembly including a novel 1.3 μm-VCSEL array and a 4-channel driver circuit is presented, its transmission performance at bit rates of 28 Gb/s and 40 Gb/s is fully investigated, and a comparison with the state of the art concerning VCSEL drivers is also discussed. Section V sums up the conclusions of the work.

II. 1.3-μM-VCSEL

A. Description

The lasers employed in Sections II and IV consist of single-mode short-cavity (SC) 1.3 μm vertical cavity surface emitting laser diodes (VCSELs). The VCSEL structure is based on Vertilas' unique InP Buried Tunnel Junction (BTJ) design (Fig. 1) and features a very short optical cavity.

Such short cavity concept has been realized by deploying dielectric materials for both the top and bottom mirror of the VCSEL, as shown in Fig. 1. In Fig. 2 the optical design of a

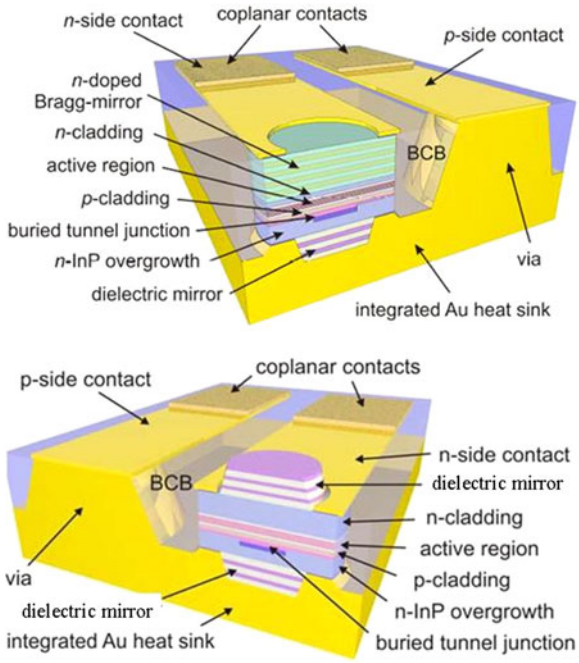

Fig. 1. Cross section of InP long-cavity (LC) and SC InP VCSEL.

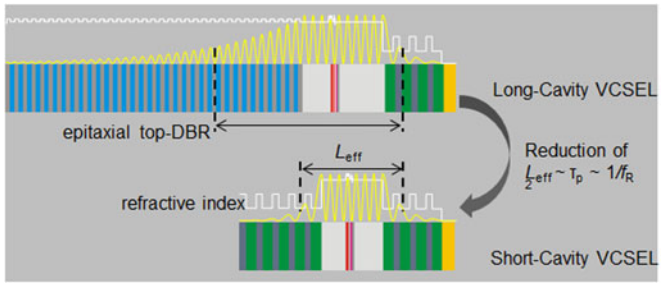

Fig. 2. Comparison of LC and SC optical VCSEL design.

long-cavity (LC) and SC VCSEL is shown, highlighting the positive effect of the reduced cavity length on the bandwidth.

As demonstrated in Fig. 2, the high refractive index of the dielectric material allows to realize a very high reflectivity distributed Bragg reflector (DBR) with only 5 mirror pairs that is much thinner compared to a semiconductor DBR with the required 30–40 mirror pairs. This reduces the effective cavity length by >30% and greatly reduces the photon lifetime, an effect that directly increases the bandwidth of the device.

The InP BTJ VCSEL concept includes a specific processing step, where most of the semiconductor material is being etched away, producing a defined semiconductor mesa structure for each laser on the wafer. The void resulting from this manufacturing step is subsequently filled with benzocyclobutene (BCB, see Fig. 1), a polymer material that is spun onto the wafer and cured under high temperatures. The mesa diameter of the latest VCSEL structure has been further optimized to reduce the device parasitics to a minimum. In addition, the active region has been improved by optimizing the number and material composition of the quantum wells and the strain. As will be shown in next sections, the optimized active region, the reduced photon

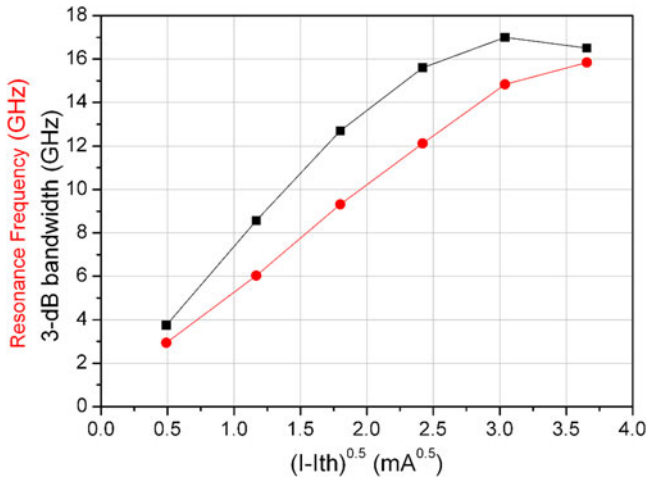

Fig. 3. Resonance frequency (black) and 3-dB modulation bandwidth (red).

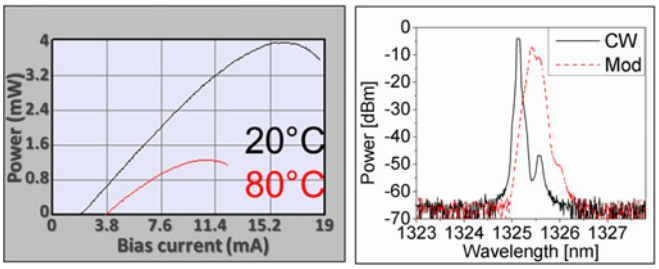

Fig. 4. Optical power versus bias current for temperature of 20 °C and 80 °C (left). Continuous wavelength (black) and 28-Gb/s modulated (dashed red) optical spectrum of the VCSEL (right).

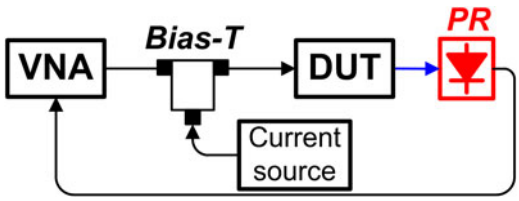

Fig. 5. Experimental setup for S21 measurement for both the die VCSEL and the transmitter assembly including FFE.

lifetime and the decreased parasitics, result in a greatly improved 3 dB-modulation bandwidth enabling direct modulation up to 40 Gb/s.

B. Characterization

As attested by the characterization shown in Fig. 3, the 1.3 μm-VCSELs exhibit a 3 dB-modulation bandwidth of up to 17 GHz (at temperature of 20 °C), which represents the highest bandwidth reported for 1.3 μm-VCSELs.

The devices also feaure excellent single-mode behavior with a side-mode suppression ratio (SMSR) $>$ 40 dB and high optical power of $\sim$4 mW at room temperature and $>$1 mW at 80 °C, as shown in Fig. 4.

S21 and, in particular, the corresponding magnitude, has been measured through the setup in Fig. 5. A vector network analyzer (VNA) applied a sweeping tone ranging from 10 MHz to 40 GHz to the device under test (DUT) that, in this case, was the die

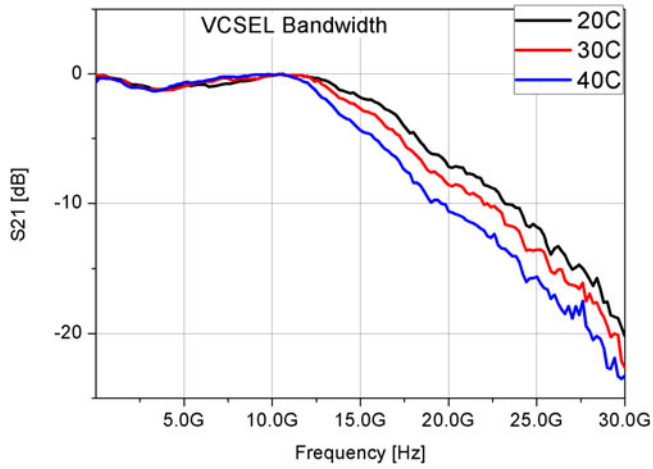

Fig. 6. S21 measurement (magnitude) of directly-modulated VCSEL for temperature ranging from 20 °C to 40 °C and bias current of 12 mA.

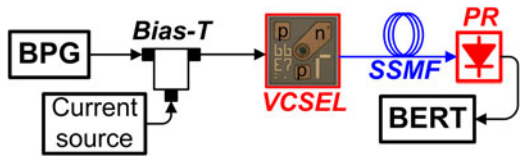

Fig. 7. Experimental setup for generation and transmission testing of 28-Gb/s OOK signal through direct modulation of the 1.3-μm VCSEL.

VCSEL. The measured S21 magnitude for temperatures equal to 20, 30 and 40 °C is plotted in Fig. 6, for a bias current of 12 mA. The corresponding 3 dB-bandwidth is 17, 15.6 and 13.8 GHz.

C. Modulation and Transmission Testing

Following its characterization, direct modulation of the laser has been tested through the setup shown in Fig. 7. An Anritsu MP1800A signal quality analyzer, including 2 bit pattern generator (BPG) modules MU181020A and a MP1821A multiplexer, is used to provide the 28 Gb/s data stream to the RF input of a high-speed bias-tee. The peak-to-peak voltage (V_{PP}) of the generated ($2^{31}-1$)–long pseudorandom bit sequence (PRBS) was set at 0.72 V, whereas to the DC input port of the bias-tee a bias current of 12 mA was applied. Light was coupled out using a cleaved single-mode fiber (SMF) pigtail in front of the VCSEL output, so as to limit optical reflections. Through a high-speed RF cable the bias-tee output signal was delivered to a signal-ground (SG) RF microprobe that was contacted to the anode (p) and cathode (n) of the VCSEL through the corresponding electrical pads (see the picture of the VCSEL layout included in Fig. 7). The device, mounted on a ceramic carrier, was placed on a Peltier cell for temperature control, enabling bit error rate (BER) measurements at different temperatures.

The obtained on-off keying (OOK) intensity-modulated signal was then transmitted along different spans of standard single-mode fiber (SSMF) G.652 whose typical zero-dispersion wavelength is in the range 1311–1321 nm.

A commercial 40G Linear PIN differential-ended Photoreceiver (DSC-R409-LW by Discovery Semiconductors, Inc.) was

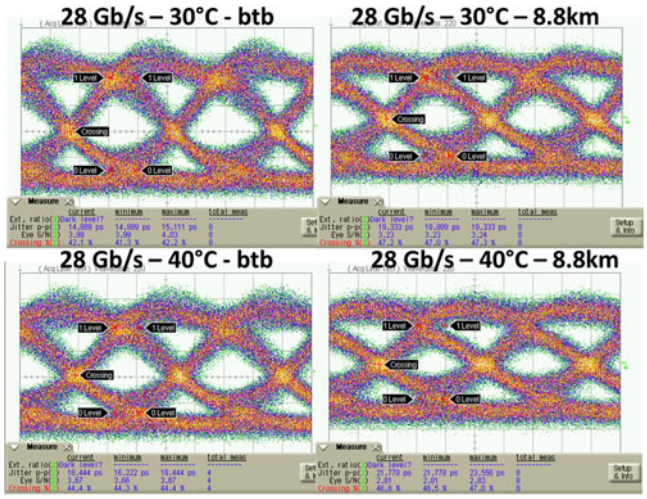

Fig. 8. Received eye diagrams at 28 Gb/s up to 8.8 km of SSMF for a temperature of 30 °C (up) and 40 °C (down), respectively.

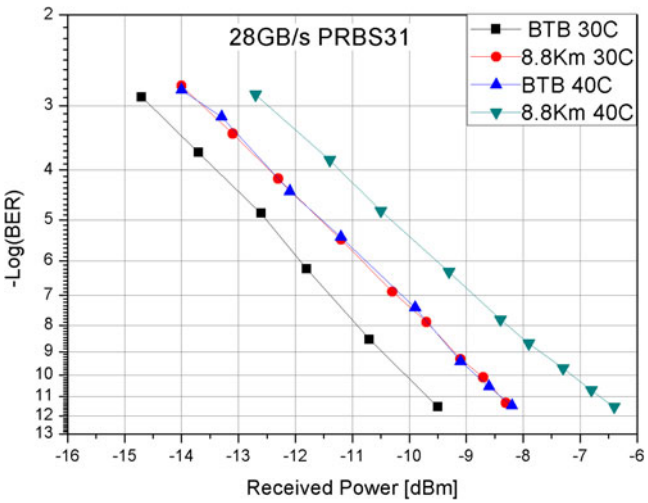

Fig. 9. BER curves versus received optical power at bit rate of 28 Gb/s for various SSMF lengths and temperature of 30 °C and 40 °C.

connected to a bit error rate tester (BERT) SHF 11100A employed for bit error rate (BER) measurements. The maximum received optical power was about −3.5 dBm in back-to-back (btb) configuration because of an extra-loss of approximately 3 dB due to the encumbrance of the RF SG microprobe when placing the cleaved SMF at the cavity output.

Fig. 8 shows eye diagrams including 220 acquired waveforms each, at the temperature of both 30 °C and 40 °C, in back-to-back (btb) configuration and after 8.8 km of SSMF (G.652) for both temperatures. Fig. 9 sums up the BER performance, demonstrating error-free operation (BER $<10^{-11}$) for each case. The maximum tested SSMF length was only due to the abovementioned available power budget. The 1.2-dB power penalty from 30 °C to 40 °C (btb) is clearly due to the decreased modulation bandwidth (Fig. 6) and that penalty is emphasized up to 1.5 dB after 8.8 km of SSMF by the combined effect of chromatic dispersion and frequency chirp. The analysis was limited to 40 °C as the experimental setup was not sufficiently stable for higher

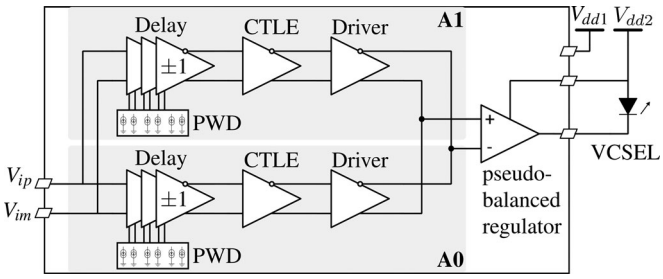

Fig. 10. Channel architecture of the driver highlighting the asymmetric two-tap FFE structure, supported by introducing adjustable PWD in each path.

temperatures. Moreover, being the measurements part of the activities within the European project RAPIDO [2], 40 °C was the agreed reference temperature for the system performance.

III. Driver Circuit

A. Description

High-speed VCSEL drivers are preferably implemented in a cathode-drive configuration to avoid slower p-type transistors in the data path. Transition times can be further improved by inserting a back-termination resistor at the output node driving the cathode [20]. However, this introduces an additional current path between the supply voltage of the driver V_{dd1} and the anode supply voltage of the VCSEL V_{dd2}. This can only be nulled by choosing V_{dd2} equal to the sum of V_{dd1} and the laser forward threshold voltage V_l, enforcing the vendor to provide multiple supply voltages. Eliminating this multi-supply voltage issue, while also guaranteeing high-speed operation was one of the main incentives for the design of the driver presented here. These features are in particular realized by the pseudo-balanced regulator, acting as the output stage of a quad channel VCSEL driver, see Fig. 10 for the channel architecture. The pseudo-balanced regulator further combines the currents at the output nodes to construct a 2-tap FFE filter response determined by tap coefficients A0 and A1. The driver block consists of an output driver and a pre-driver and is responsible for the voltage-to-current conversion.

A cascade of three delay stages controls the delay and the polarity of the pre-emphasis pulse for A0 and A1. As already demonstrated by [10], introducing explicitly pulse width distortion (PWD) in the main data path A0 can result in an asymmetric equalized response. For this design, the asymmetric behavior is further expanded by introducing PWD in the other data path A1 as well. Obtained results from experiments at 40 Gb/s in a 50 Ω environment clearly demonstrate the asymmetric pre-emphasis functionality, see Fig. 11. A continuous-time linear equalizer (CTLE) interfaces the delay stage cascade to the pre-driver and is convenient for compensating group delay variation created by the delay stages or for boosting the amplitude of a bandwidth-limited input signal. The differential input signal is delivered to the first delay stage through two 50 Ω on-chip transmission lines.

The limits of the electrical performance of the driver were tested by operating at data rates of 50 and 56 Gb/s, displayed

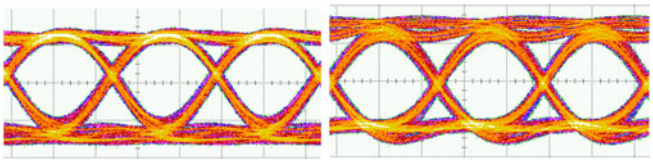

Fig. 11. Output of driver probed at 40 Gb/s with PRBS 2^7-1 while using extreme settings for PWD to demonstrate asymmetric FFE functionality (100 mV/div, 10 ps/div).

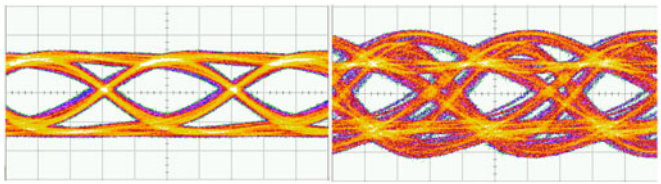

Fig. 12. Output of driver probed at 50 (left) and 56 Gb/s (right) with PRBS 2^7-1 to demonstrate the performance limitations of the driver. (100 mV/div, 5 ps/div).

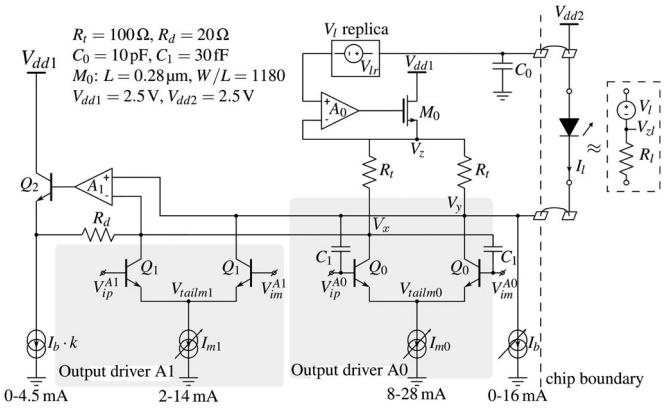

Fig. 13. Pseudobalanced regulator combining the output nodes of the FFE drivers A0 and A1.

in Fig. 12. Back-to-back (BTB) connection to the error analyzer shows a BER $< 10^{-12}$ for all three data rates while using a PRBS of 2^7-1 as input data. Transitioning to a much more critical PRBS of $2^{31}-1$ input sequence introduces a penalty at 50 Gb/s leading to a BER $> 10^{-7}$, whereas such a penalty was absent at 40 Gb/s.

B. Pseudobalanced Regulator

The current through the laser I_l can be expressed as follows for the pseudo-balanced regulator drawn in Fig. 13:

$$I_l = (I_{m0} + I_{m1} + I_b) \cdot \frac{R_t}{R_t + R_v} + \frac{V_{dd2} - V_l - V_z}{R_t + R_v}$$
$$\approx (I_{m0} + I_{m1} + I_b) \cdot \frac{R_t}{R_t + R_v} \Leftrightarrow V_z \approx V_{dd2} - V_l \approx V_{zl}$$

It consists of two terms; one determined by the current sources and the current divider ratio, while the second one represents the undesired current flow between the node voltages V_z and V_{dd2}. In a conventional cathode drive configuration, V_z resembles V_{dd1} and immediately puts a constraint on V_{dd2} if this extra current needs to be minimized. More importantly, attempting to lower V_{dd2} close to V_{dd1} negatively affects the laser current,

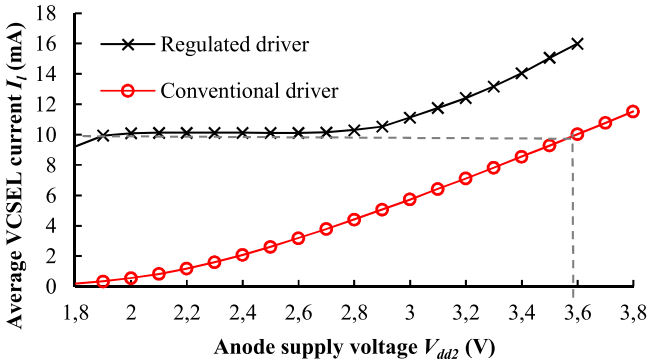

Fig. 14. Impact of anode voltage on the average VCSEL current for the same drive current is compared among the proposed regulated driver and the conventional driver circuit.

requiring a stronger contribution from the current sources and thus leading to higher power dissipation. In short, the extra current can be canceled if V_z matches internal laser node voltage V_{zl}. As V_{zl} depends on V_{dd2} and on the laser forward threshold voltage V_l, it is crucial that V_z tracks variations of both voltages. This is accomplished in the presented pseudo-balanced regulator from Fig. 13, by incorporating a linear series regulator comprising A0 and M_0 and a voltage replica V_{lr} connected to V_{dd2}.

The voltage replica is implemented as programmable V_{be}-multiplier and is set between 0.9 V and 1.1 V. The effective operation of the regulating circuit is proven in Fig. 14. The VCSEL current remains almost constant if the voltage headroom across M_0 and across the output driver A0 and A1 is sufficient, which is the case for V_{dd2} ranging from 2 V to 2.9 V. This creates the possibility for operating the VCSEL driver at a single supply voltage of 2.5 V. Above 2.9 V, the voltage regulator is not operative anymore, clearly revealing the dependency of the laser current on V_{dd2}. This dependency is especially noticeable when dealing with a conventional back-terminated driver ($V_z = V_{dd1}$) driving an equivalent non-linear VCSEL model. The exemplary targeted laser current of 10 mA can only be achieved if V_{dd2} reaches 3.6 V, unless a stronger drive current is provided resulting in a higher power consumption.

Since high-speed operation is a second important feature of the driver, several circuit additions were necessary to accommodate this. First of all, equalization is present through a 2-tap FFE, denoted by output driver A0 and A1 that are combined into the nodes Vx and Vy. A common-emitter differential pair ($Q0$, $Q1$) with a preset tail current voltage (V_{tailm0}, V_{tailm1}) was used to minimize the required headroom at the output nodes. Since this topology is heavily affected by the Miller effect, capacitors *C1* are cross-coupled to the input and output nodes of driver A0 introducing some positive feedback. The Miller effect can be mitigated by choosing *C1* slightly smaller than the base-collector capacitance of $Q0$, thereby reducing the load for the pre-driver. Secondly, as the VCSEL acts as a single-ended load for the driver, the slow dynamics of M_0 would distort the drive current to the laser. To isolate the behavior of M_0 from the output, the transient current swing through M_0 should be kept as small as possible. This is accomplished by the insertion

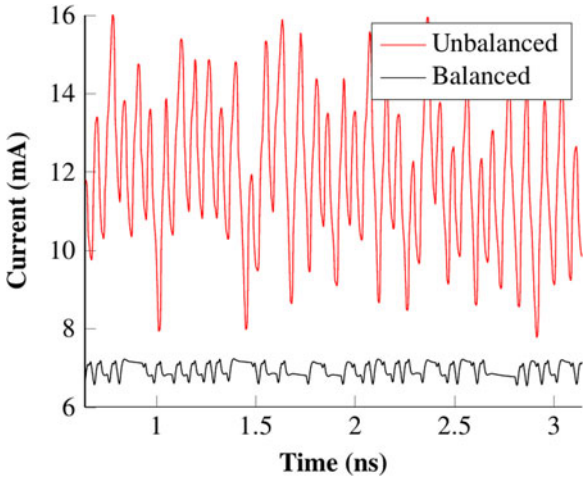

Fig. 15. Transient current flowing through node V_z has a much smaller peak-to-peak swing for the balanced configuration, compared to the unbalanced configuration.

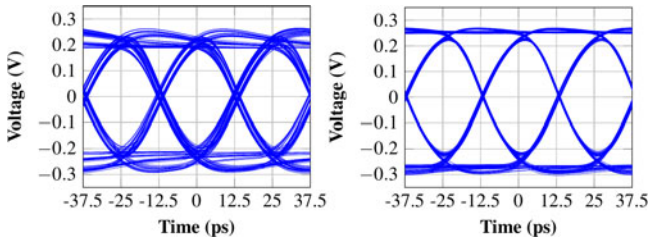

Fig. 16. 40 Gb/s $2^9 - 1$ PRBS simulation of pseudobalanced regulated output stage circuit driving a 50-Ω load (right), showing significant improvements compared to an unbalanced regulated output stage (left).

of amplifier *A1* combined with transistor *Q2* that sources a current into the dummy branch of the differential pairs to balance node *Vx* with *Vy*. A k-scaled copy of the bias current I_b is required to ensure negative feedback around transistor Q_2 under all drive conditions while dummy resistor *Rd* is added to prevent breakdown. Ideally, the transient current through transistor *M0* should be constant, something very hard to accomplish since the AC-impedance of the balancer does not match that of the VCSEL, hence the term pseudo-balancer. Nonetheless, the pseudo-balanced circuit is capable of achieving this goal quite closely after inspection of the simulated current through *M0* shown in Fig. 15, with a peak-to-peak current less than 9% of the average current. In contrast, the unbalanced topology, which is simply the same circuit from Fig. 13 but with balancer (A_1, Q_2) omitted, experiences a 65% of swing. The eye diagrams captured in Fig. 16 confirm that a large transient current swing through the converter has a detrimental impact on the high-speed performance, necessitating the use of a balancer for 40 Gb/s operation.

IV. Optical Transmitter Assembly

A. Description

The 4-channel driver integrated circuit (IC) is fabricated in a 0.13 μm SiGe BiCMOS process and measures 2.5 mm × 1.3 mm. The die is mounted on a Rogers RO4003C Lopro printed circuit board (PCB) and placed inside a cavity to reduce the length of the wire bonds towards the differential transmission lines and the VCSEL. Interfacing to 50 Ω test equipment is facilitated through 40 GHz end launch K-connectors. Since the Au substrate of the VCSEL resides on the same potential as the anode, conductive epoxy was used to directly mount the laser on the corresponding power supply trace. Power supply decoupling for both active components utilizes a mixture of external 10 to 100 nF capacitors in combination with 10 pF of on-chip capacitance for the anode voltage. The driver functionality is programmable through a serial peripheral interface bus.

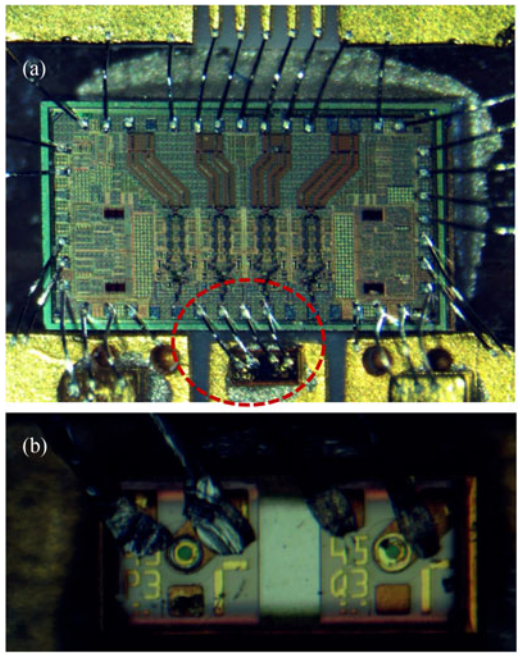

Fig. 17. (a) Wire bond assembly including the four-channel driver, wire bond to the 1 × 2 VCSEL array highlighted with red circlet. (b) Zoom of the wire bonded VCSEL array.

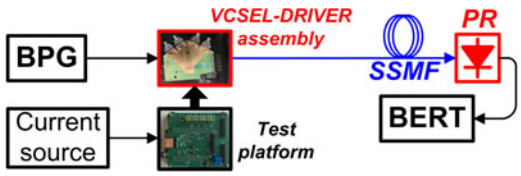

Fig. 18. Experimental setup for generation and transmission testing of 28- and 40-Gb/s OOK signal through the VCSEL-driver assembly.

B. Modulation and Transmission Testing

The assembly described in the previous section, incorporating the 4-channel driver circuit wire bonded to a 2 × 1 1325 nm-VCSEL array, was then tested by embedding it in the experimental setup shown in Fig. 18. The BPG generated two (data and inverted data) PRBS data streams with $V_{PP} = 0.6$ V that were applied in dual-drive configuration to one channel of the driver circuit included in the assembly board, through RF K-connectors. A test platform was responsible for both power supplying and programming of the VCSEL driver assembly, through a flat cable connected to the assembly. A voltage source

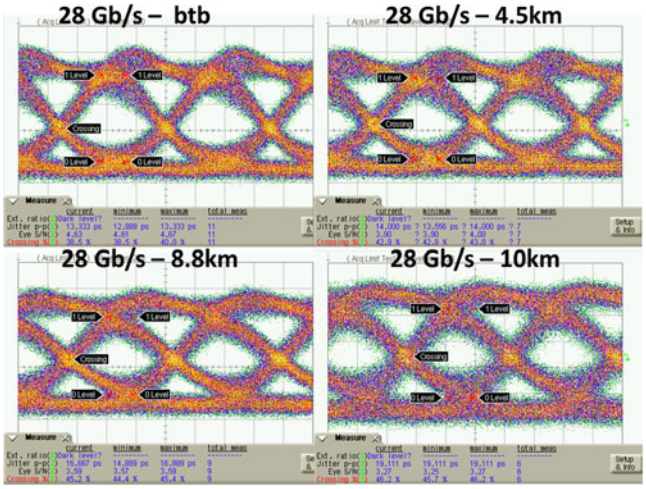

Fig. 19. Received eye diagrams up to 10 km of SSMF with the transmitter assembly, for PRBS length of $2^{31}-1$ at 28–Gb/s data rate.

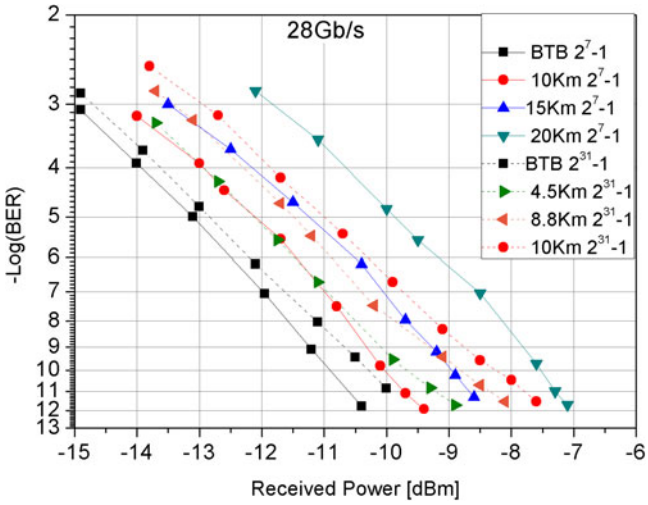

Fig. 20. BER curves versus received optical power with the transmitter assembly, at bit rate of 28 Gb/s, PRBS length of both 2^7-1 and $2^{31}-1$, for various SSMF lengths up to 10 km for PRBS31 and 20 km for PRBS7.

provided the necessary power supply to the test platform through 2.5 V-only voltages.

The transmitter assembly has been tested in uncooled condition measuring, through a thermistor, a free-run temperature *on board* of $\sim$30 °C. As described before, at that temperature the 3dB-bandwidth of a VCSEL belonging to the same wafer region than the VCSEL-array embedded in the transmitter, was measured to be 15.6 GHz (Section II-B). One of the two wire bonded channels, i.e., the rightmost one in Fig. 17(b), has been tested at first with $(2^{31}-1)$–long PRBS (PRBS31) at data rate of 28 Gb/s, similarly than in Section II-C. The provided bias current was 11 mA and, in this case, the maximum received optical power in btb configuration through the use of a cleaved SMF faced at the cavity output was about 1 dBm. This power level was possible thanks to a reduced encumbrance of the wire bond with respect to the RF probe employed in Section II-C, thus enabling a more efficient optical coupling.

Fig. 19 shows eye diagrams including 220 acquired waveforms each, for an uncooled condition, in back-to-back (btb) configuration and up to 10 km of SSMF (G.652). Extinction ratio (ER) measurement, i.e., 5.2 dB, was possible in btb only, because of the optical power level required for measuring it. Fig. 20 includes the BER performance, demonstrating error-free operation (BER $< 10^{-11}$) for each case. The maximum tested SSMF length was 10 km, exhibiting in this case a power penalty of 2.2 dB with respect to the btb case, with a residual power budget of 3.2 dB (received power equal to -4.4 dBm).

As in previous demonstrations direct modulation of VCSEL was proved to be sensitive to the pattern length [6], [24], the transmission performance has been tested for PRBS7 too. The corresponding eye diagrams have been shown in Fig. 21 for various SSMF lengths up to 20 km. The BER performance are included in Fig. 20 demonstrating error-free operation for all SSMF lengths and, in particular, attesting 3.3 dB-power penalty after 20 km of SSMF with residual power budget of 1.6 dB. Fig. 21 also shows the eye diagram in btb configuration when disabling the FFE functionality, i.e., with only 1 tap applied,

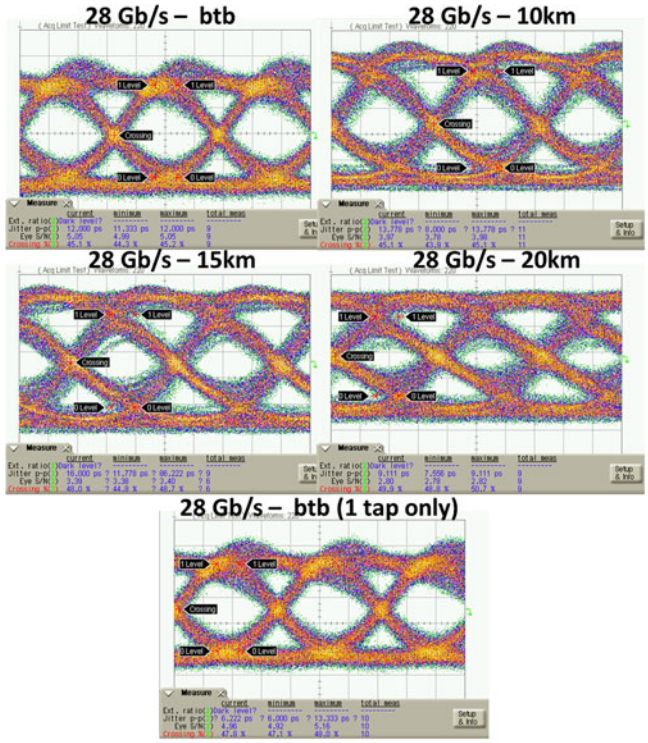

Fig. 21. Received eye diagrams up to 20 km of SSMF with the transmitter assembly, for PRBS length of 2^7-1 at 28-Gb/s data rate.

demonstrating a modest impact of the 2-tap equalization at 28 Gb/s. Indeed BER measurements for this case have not been included in Fig. 20 as they look basically identical to the 2-tap case (maximum deviation from 2-tap case within 0.2 dB).

The performance of the transmitter assembly has been finally tested for a data rate of 40 Gb/s (in this case 4 BPG modules MU181020A have been used). The setup was identical to the 28 Gb/s case, except for the differential driver input. Indeed, due to the limited phase matching specifications of the employed RF cable pair, not guaranteeing efficient differential driving

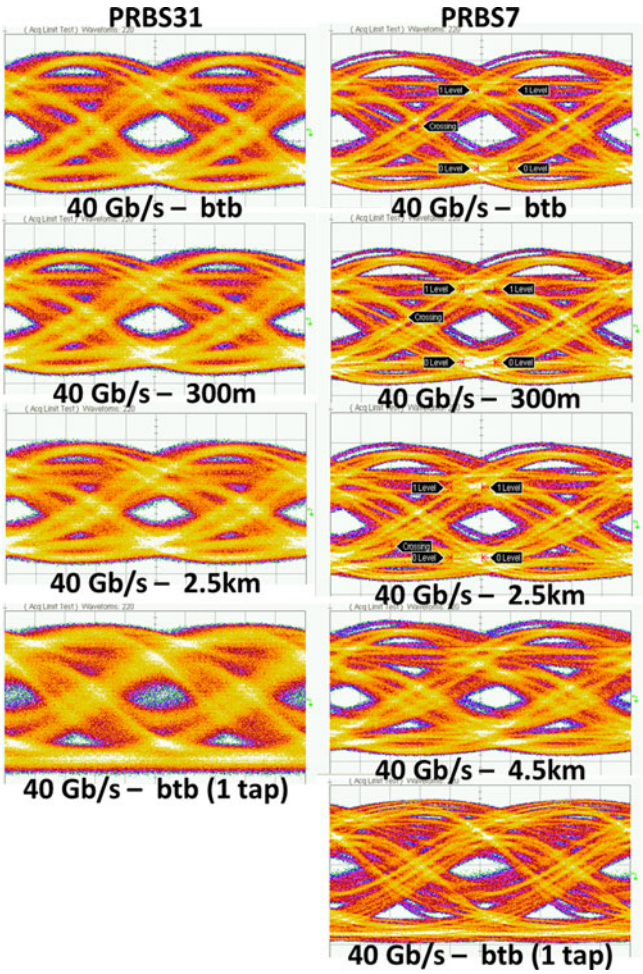

Fig. 22. Received eye diagrams at 40 Gb/s for both PRBS31 and PRBS7, up to 2.5 and 4.5 km of SSMF respectively, including the one-tap case for both pattern lengths.

operation at 40 Gb/s, only single-ended input drive was applied at 40 Gb/s.

Again the transmitter has been tested for both PRBS31 and PRBS7 data streams with bias current equal to 12 mA. Eye diagrams in both cases have been shown in Fig. 22 up to 2.5 km and 4.5 km of SSMF respectively, measuring an ER of 2.8 dB in btb configuration. For each PRBS length, the figure also includes the btb eye diagram in case of no equalization (1-tap case), to demonstrate the crucial benefit of FFE at 40 Gb/s. In particular, a completely closed eye diagram can be noticed without equalization for PRBS31. The different appearance of 40 Gb/s eye diagrams with respect to those at 28 Gb/s (Figs. 8, 19, and 21) is due to the use of a precision timebase module (Agilent 86107A) for clock triggering, which leaded to a much longer time (minute range) required to acquire 220 waveforms. The employed sampling oscilloscope for eye diagrams visualization was an Agilent 86100A (50G 86109B module). Fig. 23 sums up BER performance at 40 Gb/s. For PRBS7 error-free operation (BER $< 10^{-11}$) was achieved with sensitivity of -4.9 dBm, with 1.5 dB-penalty after 4.5 km of SSMF and residual power budget of 3.2 dB. In case of PRBS31 a clear floor behavior (partly enhanced by the log-log vertical scale in Fig. 23)

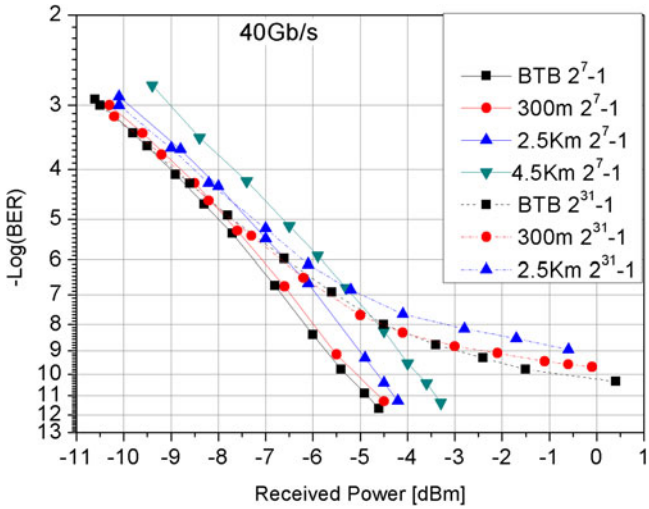

Fig. 23. BER curves versus received optical power of the transmitter assembly, at bit rate of 40 Gb/s, PRBS length of both 2^7-1 and $2^{31}-1$, for various SSMF lengths up to 2.5 km for PRBS31 and 4.5 km for PRBS7.

of all BER curves is evident; a minimum BER $= 4.5 \cdot 10^{-11}$ was achieved in btb and increases up to $1.1 \cdot 10^{-9}$ after 2.5 km of SSMF, with a power penalty of 2.5 dB ($@BER \sim 10^{-9}$).

The notable impact of the pattern length, particularly detrimental when stressing the operation up to 40 Gb/s, is addressed in the next section.

C. S21 Measurements

In order to investigate the effectiveness of the 2-tap FFE implemented through the BiCMOS driver circuit, the modulation bandwidth has been attested in various conditions, i.e., with and without FFE, through S21 measurements.

Referring to the setup shown in Fig. 5, the DUT was here the transmitter assembly. The die VCSEL, whose S21 at various temperatures was reported by Fig. 6, and the two VCSELs included in the 1×2 array bonded into the assembly present the same structure, come from the same wafer region and exhibited equivalent static performance concerning diode voltage and output optical power versus diode current.

Fig. 24 shows S21 (magnitude) measurements of the transmitter assembly with and without 2-tap FFE in comparison with S21 of the die VCSEL for temperatures of 20 °C and 30 °C, that was already shown in Fig. 6. Even though the benefit in terms of 3 dB-bandwidth is evident in the frequency range 12 GHz–22 GHz when applying FFE (2 taps), a quite evident higher-order frequency response and corresponding steeper behavior appears at higher frequencies for the driver assembly. This is mainly caused by the wire bond inductance that introduces an extra pole by reacting with the electrical parasitics of the driver and the VCSEL. A phenomenon not present when probing the die VCSEL. As the free-run temperature of the assembly was ~30 °C, in comparison with S21 of the die VCSEL for that temperature also the 1-tap case exhibits a larger 3 dB-bandwidth in the same abovementioned frequency range. Indeed the 1-tap case retraces the 20 °C case, which presents a higher bandwidth than the 30 °C case, up to 20 GHz. For frequencies

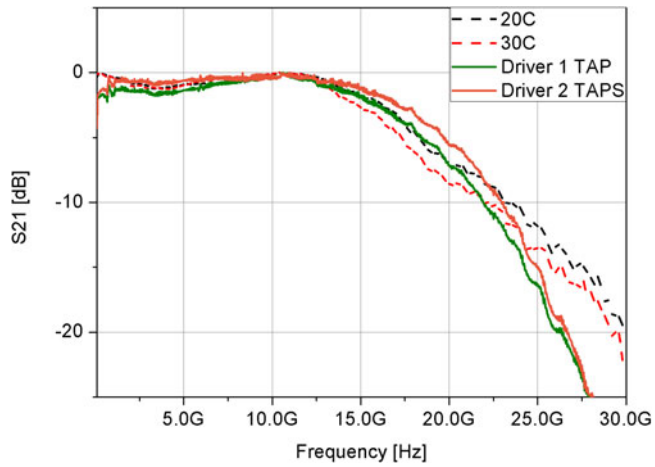

Fig. 24. S21 measurement of the die VCSEL for temperatures of 20 and 30 °C and of the transmitter assembly with/without two-tap FFE.

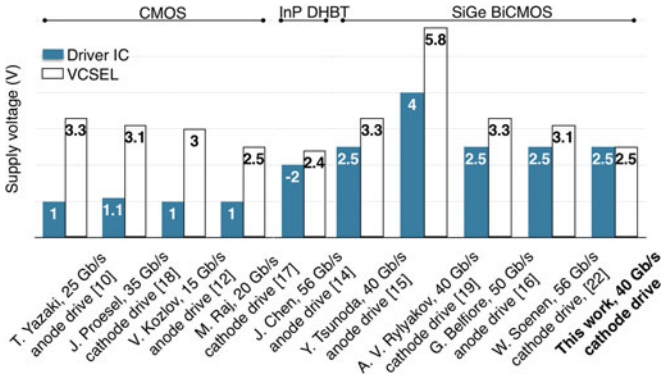

Fig. 25. Comparison of supply voltages powering state-of-the-art VCSEL drivers for multiple transistor technologies and drive configurations.

higher than 22 GHz and 24.5 GHz, S21 without driver circuit outperforms respectively the 1-tap and 2-tap case. The higher 3 dB-bandwith with 2 taps with respect to 1 tap only confirms the benefit obtained through FFE in case of 40 Gb/s operation, together with the larger dip at low frequencies (< 8 GHz) in case of 1 tap only. Even though such dip gets partly reduced through FFE with respect to 1 tap (and to the die VCSEL too), it might explain the performance degradation for longer pattern lengths. Indeed PRBS31 includes identical bit sequences as long as up to 30 bits, reaching frequency contents down to 1.33 GHz in case of 40 Gb/s and 933 MHz incase of 28 Gb/s. This aspect in combination with the limited modulation bandwidth (18 GHz for 2-tap FFE) might lead to the floor exhibited by BER curves in Fig. 23 in case of PRBS31. The degradation due to the low-frequency dip should have an higher impact at 28 Gb/s but, at the same time, the less stringent modulation bandwidth limitation could be the reason for a less pronounced penalty on the BER at 28 Gb/s with respect to the 40 Gb/s case.

D. Comparison With State-of-the-Art VCSEL Drivers

The primary targets of the presented driver circuit are to achieve low-power high-speed operation while operating via a single supply voltage for both electrical and optical devices. As can be seen in Fig. 25, it definitely excels in terms of the last target as the maximum required supply remains below anode drive CMOS implementations.

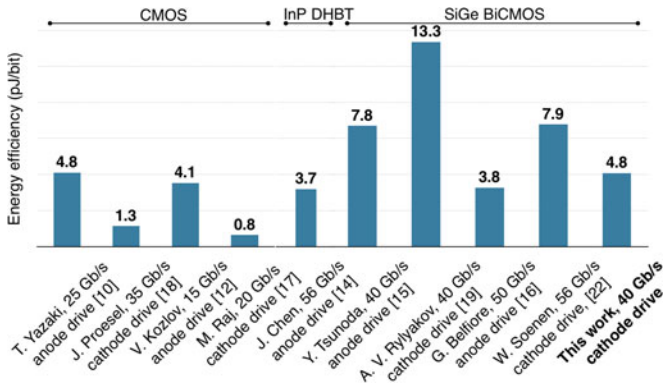

Fig. 26. Comparison of energy efficiency of state-of-the-art VCSEL drivers for multiple transistor technologies and drive configurations.

The measured power consumption of the whole assembly was ~190 mW, of which 170 mW was consumed by the driver and FFE and ~20 mW was required for VCSEL biasing. This translates into an energy-per-bit of 4.75 pJ/bit at 40 Gb/s, which can certainly compete with SiGe and InP bipolar transistor and bulk CMOS transistor driver designs (Fig. 26).

In addition, the potential of the presented 1.3 μm BTJ VCSEL driver assembly for data center and inter-data center traffic is strongly supported by comparing its efficiency with respect to similar solutions, through the energy-to-data-ratio per km, as figure of merit. Error-free and digital signal processing (DSP)-free transmission at 28 Gb/s over 20 km of SSMF leads to 29 fJ/bit/km, whereas, concerning 1.3 μm solutions, in [8] 119 fJ/bit/km at 25 Gb/s over 10 km of SMF can be deduced and, concerning 1.55 μm solutions, in [25] 57 fJ/bit/km are required excluding DSP power consumption to achieve a BER $< 10^{-6}$ at 28 Gb/s over 10 km of SSMF.

V. Conclusion

An optical transmitter supporting both 28 Gb/s and 40 Gb/s data rates per channel (wavelength) based on on-off keying direct intensity modulation of 1.3 μm-VCSEL has been presented. The assembly incorporates a 0.13 μm SiGe BiCMOS 4-channel driver circuit including feed forward equalization functionality, wire bonded to a 2×1 1325 nm-VCSEL array. Capability of transmitting over distances multiple times longer than using 1.55 μm devices has been demonstrated at both 28 Gb/s and 40 Gb/s data rates in uncooled condition (free-run temperature of about 30 °C). In particular error-free (EF) operation (BER $< 10^{-11}$) has been demonstrated up to 20 km and 4.5 km of standard single-mode fiber (SSMF) respectively for the two data rates, for (2^7-1)–long pseudorandom bit sequence (PRBS7). Performance for PRBS31 has been attested to reach EF operation up to 10 km of SSMF at 28 Gb/s and a minimum BER $\sim 10^{-9}$ up to 2.5 km of SSMF at 40 Gb/s. The degradation of performance in case of applying long identical-bit sequences can be easily bypassed through the use of a number of coding techniques, such as 8 b/10 b encoding [26]. The transmitter exhibits state-of-the-art energy consumption per bit, i.e., 4.75 pJ/bit at 40 Gb/s, as well as energy-to-data-ratio per km of

29 fJ/bit/km (considering 28 Gb/s over 20 km of SSMF) which is a value outperforming similar VCSEL driver solutions. The achieved results, especially in terms of fiber reach, make the proposed transmitter suitable not only for short-reach applications, but also for up to the access segment. In addition, the 4-channel driver chip employed with quad VCSEL-array is a solution that might support 100 or even 160 Gb/s VCSEL link, in the first case being compliant with the IEEE 802.3 100 GBASE LR4 standard (10 km SSMF, 4×25 Gb/s).

REFERENCES

[1] M. Ortsiefer *et al.*, "Long wavelength high speed VCSELs for long haul and data centers," in *Proc. Opt. Fiber Commun. Conf.*, San Francisco, CA, USA, 2014, Paper W4C.2.

[2] T. Aalto *et al.*, "Integrating III-V, Si, and polymer waveguides for optical interconnects: RAPIDO," *Proc. SPIE*, vol. 9753, May 24, 2016, Art. no. 97530D.

[3] D. M. Kuchta *et al.*, "Error-free 56 Gb/s NRZ modulation of a 1530-nm VCSEL link," *J. Lightw. Technol.*, vol. 34, no. 14, pp. 3275–3282, Jul. 15, 2016.

[4] S. Spiga *et al.*, "Single-mode high-speed 1.5-μm VCSELs," *J. Lightw. Technol.*, vol. 35, no. 4, pp. 727–733, Feb. 15, 2017.

[5] W. C. Soenen *et al.*, "A 40-Gb/s 1.5-μm VCSEL link with a low-power SiGe VCSEL driver and TIA operated at 2.5 V," in *Proc. Opt. Fiber Commun. Conf. Exhib.*, Los Angeles, CA, USA, 2017, Paper Th3G.4.

[6] A. Malacarne *et al.*, "Performance analysis of 40-Gb/s transmission based on directly modulated high-speed 1530-nm VCSEL," *IEEE Photon. Technol. Lett.*, vol. 28, no. 16, pp. 1735–1738, Aug. 15, 2016.

[7] [Online]. Available: http://www.ieee802.org/3/bs/public/14_05/ghiasi_t3bs_01b_0514.pdf

[8] A. Caliman *et al.*, "25 Gbps direct modulation and 10 km data transmission with 1310 nm waveband wafer fused VCSELs," *Opt. Express*, vol. 24, pp. 16329–16335, 2016.

[9] M. Muller *et al.*, "1.3 μm short-cavity VCSELs enabling error-free transmission at 25 gbit/s over 25 km fibre link," *Electron. Lett.*, vol. 48, no. 23, pp. 1487–1489, 2012.

[10] T. Yazaki, N. Chujo, H. Yamashita, T. Takemoto, Y. Lee, and Y. Matsuoka, "25-Gbps $\times$ 4 optical transmitter with adjustable asymmetric pre-emphasis in 65-nm CMOS," in *Proc. IEEE Int. Symp. Circuits Syst.*, Melbourne, VIC, Australia, 2014, pp. 2692–2695.

[11] D. Kucharski *et al.*, "A 20 Gb/s VCSEL driver with pre-emphasis and regulated output impedance in 0.13 μm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, San Francisco, CA, USA, 2005, vol. 1, pp. 222–594.

[12] V. Kozlov and A. Chan Carusone, "Capacitively-coupled CMOS VCSEL driver circuits," *IEEE J. Solid-State Circuits*, vol. 51, no. 9, pp. 2077–2090, Sep. 2016.

[13] L. Szilagyi, G. Belfiore, R. Henker, and F. Ellinger, "30 Gbit/s 1.7 pJ/bit common-cathode tunable 850-nm-VCSEL driver in 28 nm digital CMOS," in *Proc. IEEE Opt. Interconnects Conf.*, Santa Fe, NM, USA, 2017, pp. 51–52.

[14] J. Chen *et al.*, "An energy efficient 56 Gbps PAM-4 VCSEL transmitter enabled by a 100 Gbps driver in 0.25 μm InP DHBT technology," *J. Lightw. Technol.*, vol. 34, no. 21, pp. 4954–4964, Nov. 1, 2016.

[15] Y. Tsunoda, M. Sugawara, H. Oku, S. Ide and K. Tanaka, "8.9 A 40 Gb/s VCSEL over-driving IC with group-delay-tunable pre-emphasis for optical interconnection," in *Proc. IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, San Francisco, CA, USA, 2014, pp. 154–155.

[16] G. Belfiore, M. Khafaji, R. Henker, and F. Ellinger, "A 50 Gb/s 190 mW asymmetric 3-tap FFE VCSEL driver," *IEEE J. Solid-State Circuits*, vol. 52, no. 9, pp. 2422–2429, Sep. 2017.

[17] M. Raj, M. Monge, and A. Emami, "A modelling and nonlinear equalization technique for a 20 Gb/s 0.77 pJ/b VCSEL transmitter in 32 nm SOI CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 8, pp. 1734–1743, Aug. 2016.

[18] J. E. Proesel, B. G. Lee, C. W. Baks, and C. L. Schow, "35-Gb/s VCSEL-based optical link using 32-nm SOI CMOS circuits," in *Proc. Opt. Fiber Commun. Conf. Expo./Nat. Fiber Opt. Eng. Conf.*, Anaheim, CA, USA, 2013, Paper OM2H.2.

[19] A. V. Rylyakov *et al.*, "A 40-Gb/s, 850-nm, VCSEL-based full optical link," in *Proc. Opt. Fiber Commun. Conf. Expo./Nat. Fiber Opt. Eng. Conf.*, Los Angeles, CA, USA, 2012, Paper OTh1E.1.

[20] D. M. Kuchta *et al.*, "A 56.1 Gb/s NRZ modulated 850 nm VCSEL-based optical link," in *Proc. Opt. Fiber Commun. Conf. Expo. /Nat. Fiber Opt. Eng. Conf.*, Anaheim, CA, USA, 2013, Paper OW1B.5.

[21] D. M. Kuchta *et al.*, "A 71-Gb/s NRZ modulated 850-nm VCSEL-based optical link," *IEEE Photon. Technol. Lett.*, vol. 27, no. 6, pp. 577–580, Mar. 15, 2015.

[22] W. Soenen *et al.*, "56 Gb/s PAM-4 driver IC for long-wavelength VCSEL transmitters," in *Proc. 42nd Eur. Conf. Opt. Commun.*, Dusseldorf, Germany, 2016.

[23] A. Malacarne *et al.*, "Low-power 1.3-μm VCSEL transmitter for data center interconnects and beyond," in *Proc. 43rd Eur. Conf. Opt. Commun.*, Gothenburg, Sweden, 2017, Paper M.2.C.5.

[24] W. Hofmann *et al.*, "40 Gbit/s modulation of 1550 nm VCSEL," *Electron. Lett.*, vol. 47, no. 4, pp. 270–271, Feb. 17, 2011.

[25] F. Karinou, N. Stojanovic, A. Daly, C. Neumeyr, and M. Ortsiefer, "1.55-μm long-wavelength VCSEL-based optical interconnects for short-reach networks," *J. Lightw. Technol.*, vol. 34, no. 12, pp. 2897–2904, Jun. 15, 2016.

[26] A. X. Widmer and P. A. Franaszek, "A DC-balanced, partitioned-block, 8 B/10 B transmission code," *IBM J. Res. Develop.*, vol. 27, no. 5, pp. 440–451, 1983.

Authors' biographies not available at the time of publication.