Linear–Logarithmic CMOS Pixel With Tunable Dynamic Range

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Abstract—A CMOS pixel with linear–logarithmic response and programmable dynamic range (DR), based on a tunable transition point, has purposely been designed for endoscopic applications. A theoretical model of the pixel was developed and validated. A chip with a 100×100 pixel array and a 12-b digital output was fabricated in a 0.35-μm technology and was fully tested, thus demonstrating state-of-the-art performance in terms of DR and noise. Intraframe DR proved to be extendable to more than 110 dB through a logarithmic compression of the signal in the light irradiation power density (LIPD) range. The measured temporal noise (pixel noise) was less than 0.22% over the full range. The architecture presented limited fixed pattern noise (FPN) due to the scheme adopted, which allowed its correction over the full signal range: FPN was 0.83% (1.37%) in the linear (logarithmic) region. Although the test chip was designed mainly for endoscopic applications, the technology may also be applied to other fields, e.g., robotics, security and industrial automation, whenever high DR is a crucial feature.

Index Terms—CMOS imager, endoscopy, logarithmic response, pixel.

I. INTRODUCTION

SINCE 1879 [1], vision systems have widely been used in biomedical applications, mainly for endoscopic inspection and visualization enhancement in surgery. Despite this condition, the first fiber endoscope was developed more than 70 years later when Hopkins and Kapani published the use of a gastroscope based on coherent glass fibers in 1954 [2]. One additional milestone was reached in this field with the introduction of television, which allowed binocular vision from a convenient distance by several observers. In 1988, a digital vision system that was placed on the distal part of the instrument eliminated the need for optical fibers that run through the entire shaft [1]. Nowadays, as a consequence of the wide diffusion of minimally invasive diagnostic and surgical techniques, endoscopic vision systems have dramatically strengthened their role in the surgical field [3], [4].

Minimally invasive surgery allows surgeons to perform procedures through small incisions, thereby offering several benefits to the patient, e.g., reduced trauma and faster recovery, compared to traditional open techniques. Since its introduction, surgical endoscopy has played a major role in improving the safety, precision, and reliability of medical interventions. The most desirable features of an endoscopic vision system are high image resolution, low noise, bright illumination, and low working temperature. Saturated regions must particularly be prevented, because they limit and, sometimes, hamper image comprehension.

The disruptive progress that was achieved by the CMOS imager industry in the last few years, mainly driven by consumer electronics, has allowed all these requirements to simultaneously be met [5]. This case is particularly true for saturation, which can be prevented by using high-dynamic-range (HDR) image sensors [6].

HDR image sensors allow a wide range of light irradiation power density (LIPD) to be mapped in the same picture. Techniques for obtaining HDR have widely been investigated and can be classified as interframe and intraframe techniques. In the former case, images are combined together to obtain a single HDR image [7]–[10], whereas in the latter case, the whole light dynamic is mapped in the same image.

With regard to the interframe approach, the multi-integration technique is currently the most commonly used approach at the industrial level, because it is based on a simple concept. In particular, this approach is easily implementable with a CMOS sensor.

Among existing intraframe techniques, the simplest approach is the logarithmic technique [11], [12]. The array is continuously read out and the photodetector output is compressed with a dynamic metal–oxide–semiconductor field-effect transistor (MOSFET) load. This case results in a logarithmic relationship between the LIPD input and the voltage output covering more than six decades of LIPD. The main advantages of this technique are its simple architecture and HDR. On the other hand, poor response at low light intensity and high residual fixed pattern noise (FPN) are the main drawbacks.

One alternative and more recent technique for obtaining intraframe HDR is the time-to-saturation approach [13]. In this case, the output is obtained by combining a standard linear output and a signal related to the time required by the photodiode to saturate. The DR can be extended to more than 120 dB, depending on the function used to map the saturation time into the output voltage. A detailed reference list with a comparative theoretical study of main HDR architectures is reported in [14].

Focusing on endoscopic applications, the main requirements for an HDR vision system are chip size and image quality. Consequently, the cited techniques could hardly be implemented in endoscopy. In fact, the multi-integration technique is based on the acquisition of the same image, with different integration times, to obtain an HDR image from their superposition. This case is not always guaranteed during endoscopic inspections because of possible movements (e.g., peristalsis, respiration, and tool motion) during image acquisition. With regard to intraframe techniques, the time-to-saturation pixel guarantees good image quality, at the cost of a relevant pixel pitch. Therefore, high resolution cannot be achieved, unless a large silicon area is used. The logarithmic pixel is an intraframe approach that can be implemented in a small pitch; however, the response at low LIPD is poor. This condition is a crucial drawback in the event of a light- and temperature-controlled environment, e.g., endoscopy.

Based on these considerations, a novel image sensor with linear–logarithmic response was developed by merging the simple design and the HDR of the logarithmic technique in case of high LIPD with a linear response at low intensity light. This case is not the first time that a linear–logarithmic pixel is presented in the literature [15]. The main innovative feature of the proposed design consists of the integration of a hard reset structure that gives rise to an FPN subtraction in hardware—completely when the response is in the linear region and partially when the behavior is logarithmic. Moreover, the power responsivity curve can be adjusted through a tunable analog reference to dynamically achieve the desired tradeoff between HDR and high pixel resolution [16], [17].

To preliminarily evaluate the performance of this new pixel architecture, one model of the pixel response was developed and is presented in Section II. The new technique was implemented in a 100×100 pixel image sensor, fabricated in a standard 0.35-μm, 3.3-V CMOS technology. Details are given in Section III. Section IV gives concrete information on performance by illustrating the results of the electro-optical tests that were carried out and by comparing them to the proposed model. This section also describes the performance of endoscopic image acquisition through *ex vivo* experiments.

II. PIXEL ARCHITECTURE AND MODEL

The linear–logarithmic pixel that was integrated in the proposed chip is shown in Fig. 1. The core is the same as that of a linear pixel. The photodiode (D1), a first MOSFET that works as a reset switch (M1), and a second MOSFET (M5), in source–follower configuration, shield the photosensitive node from the load of the readout chain. A global shutter (SH), which consists of a transistor (M4) that was driven by an external signal, completes the basic block. Note that, during preliminary testing, the sensitivity of the pixel was relevantly affected by the switching of the M4 transistor. Therefore, it was excluded from the signal chain by leaving it always switched on and will not be considered in the following discussion. HDR functionality is guaranteed by a series of transistors (M2 and M3), with the gate connected to the drain in a diode configuration. Placing a second transistor in series to the first one doubles the gain in
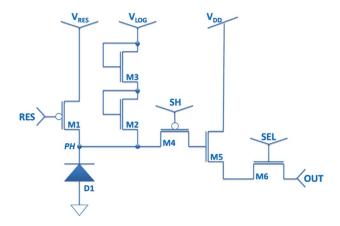

Fig. 1. Schematic of the linear–logarithmic pixel.

the logarithmic region, thus enhancing the signal-to-noise ratio (SNR) [18].

This part of the circuitry works as a voltage-light dependent active load, and is responsible for the logarithmic compression. Such a load is active only when the voltage V_{PH} at the photosensitive node (PH) exceeds a threshold which can be tuned by the operator through an external reference voltage V_{LOG}.

The operation of the pixel starts with a *reset status*. During this phase, the reset transistor M1 is switched on, and the photosensitive node (PH) is pulled to the reference voltage V_{RES}, which can be adjusted by the user. The following *integration phase* begins with the release of PH by switching M1 off. PH is now isolated. and its voltage (V_{PH}) starts to decrease as a consequence of the charge carriers drained by the photogenerated current. The higher the photosensitive current is, the faster the discharge will be. If the combination of light intensity and integration time is not enough to allow the pixel to reach the threshold at which the active load starts to work (i.e., $V_{\text{LOG}} - 2^{*}V_{\text{TH}}$, where V_{TH} is the transistor threshold voltage, then the signal V_{PH} at the photosensitive node will be proportional to the photogenerated current (i_{PH}), increased by the dark current (i_{dark}), and to the integration time (t_{INT}) as follows [6]:

$$V_{\text{PH}} = \frac{t_{\text{INT}}(i_{\text{PH}} + i_{\text{dark}})}{C_{\text{IN}}} \quad V_{\text{PH}} > V_{\text{LOG}} - 2^{*}V_{\text{TH}} \quad (1)$$

where C_{IN} is the capacitance at the photosensitive node, which is made up of the intrinsic photodiode capacitance and the parasitic one.

If V_{PH} reaches the threshold that was tuned by V_{LOG}, then the active load starts to work by draining part of the photogenerated current. The result is a logarithmic relation between i_{PH} and V_{PH}.

This behavior is obtained due to the subthreshold working condition of the M2 and M3 load transistors, guaranteed by the shortcut between the gate and the drain ($V_{\text{GS}} = V_{\text{DS}}$). Indeed, for $V_{\text{DS}} < V_{\text{TH}}$, the transistor should be switched off. However, from an analog standpoint, the transistor is in weak inversion, and a small current of minority carriers (i_D) flows in the MOSFET channel.

The equation for i_{DS} is [19]

$$i_{DS} = D_n \frac{kT}{\sqrt{\frac{2qN_A\Psi_S}{\varepsilon_{Si}}}} \left(\frac{W}{L}\right) \left(\frac{n_i^2}{N_A}\right) e^{\frac{q\Psi_S}{kT}} \left(1 - e^{-\frac{qV_{DS}}{kT}}\right)$$

$$(2)$$

where n_i and N_A are, respectively, the intrinsic and the donor doping concentration, Ψ_s is the surface potential, ϵ_{Si} is the silicon dielectric constant, W and L are the MOSFET width and length, and D_n is the electron diffusivity. At room temperature, $V_{DS} > 3kT/q \sim 75$ mV, and the last term of this equation is around 1. Furthermore, $V_{DS} = V_{GS} = n\Psi_S$, and all the constant parts of the formula can be collected in one single term as

$$i_0 = D_n \frac{kT}{\sqrt{\frac{2qN_A\Psi_S}{\varepsilon_{Si}}}} \left(\frac{W}{L}\right) \left(\frac{n_i^2}{N_A}\right)$$

$$(3)$$

where $D_n = (kT/q)\mu_n$, and μ_n is the electron mobility.

Therefore, (2) can be simplified as

$$i_{DS} = i_0 e^{\frac{V_{DS}}{\frac{kT}{q}}}.$$

$$(4)$$

This formula can be inverted to find the source voltage as logarithmically dependent on the i_{DS} current. We have

$$V_S = V_D - (kT/q)^* \ln(i_{DS}/i_0)$$

$$(5)$$

with $V_S = V_{PH}$, $V_D = V_{LOG}$, and $i_{DS} = i_{PH}$. Equation (5) represents the logarithmic relation between the photogenerated current and the voltage at the photosensitive node for a single transistor load and for $V_{PH} \geq V_{LOG} - V_{TH}$. In the configuration presented in Fig. 1, the load transistors are M1 and M2, and the transfer function in the logarithmic region is

$$V_{PH} = V_{LOG} - 2^*(kT/q)^* \ln(i_{DS}/i_0) \quad V_{PH} \leq V_{LOG} - 2^*V_{TH}.$$

$$(6)$$

To relate these results to the physical implementation presented in this paper, the electrical design rules from ON-Semiconductor (formerly AMI) 0.35 μm [20] may be considered. This standard CMOS technology was chosen for the proposed sensor, because it may partially be customized, thus enhancing the overall sensor performance. In particular, a nonstandard shield to silicide implant and to complementary p-well diffusion was added at the array level [21].

To define a model that can practically be used, a series of approximations must be assumed. In particular, i_0, which is temperature dependent as T^2 [11], is considered constant over the whole temperature range. This assumption is acceptable for endoscopic applications, where the temperature is supposed to be constant. As a result, based on the data from the silicon foundry, the i_0 current is in the order of 0.01 fA, and the logarithmic response may be calculated as a function of the photogenerated current.

The model was developed by using Microsoft Excel 2007, and the results are shown in Fig. 2. As further reported, the model was validated on the developed prototype. Once
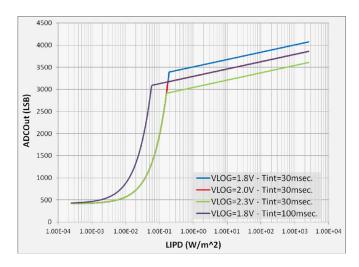

Fig. 2. Simulated power responsivity for the linear–logarithmic pixel at different V_{LOG} and T_{INT} values. ADCOUT is the ADC digital output word as defined in Section III.

experimentally verified, the model will allow the theoretical extrapolation of several parameters that would otherwise be difficult to measure, e.g., the capacitance at the photosensitive node and the actual dark current.

As shown in Fig. 2, the response in the logarithmic region maintains the same trend, regardless of the integration time. In particular, V_{PH} is not affected by C_{IN} [see (5)]. This condition leads us to conclude that the DR is not related to the full-well capacitance, as in linear pixels, but is potentially limited only by the voltage range of the readout channel and the silicon secondary effects. The C_{IN} effect is only relevant for the linear region, where a small C_{IN} value would increase the slope of the power responsivity, as highlighted in (1), thus resulting in an improved discrimination between different levels of input signal. To better fit the linear region, a dependency of the photodiode capacitance from the applied voltage was considered in C_{IN} [6]. This approach results in a better fit in the low-light region.

III. IMPLEMENTATION OF THE PIXEL IN A TEST CHIP

The linear–logarithmic technique presented in this paper was implemented in a monolithic active-pixel gray-level camera-on-a-chip sensor. The photo-sensitive matrix consists of a 100×100 pixel array based on an n-well/p-substrate photo-diode, with a pixel pitch of 9.4 μm $\times$ 9.4 μm and a fill factor (FF) of 30% [6]. The sensor integrates a pixel array, a number of column data sampling (CDS) blocks, a data double sampling (DDS) block at the array level [10] with double sampling and preamplification capability, a 12-b analog-to-digital converter (ADC), and several other support blocks (see Fig. 3).

When a row-decoder addresses a row, every pixel of the selected line simultaneously transfers its output value to a CDS, which stores the information. Then, the pixels of the selected row are reset, and their reset values are transferred to the associated bit-line CDS. The CDS subtracts this value from the stored one and makes the result available at the output. This subtraction between two noncorrelated samples mainly allows pixel FPN reduction. Depending on the response, either linear
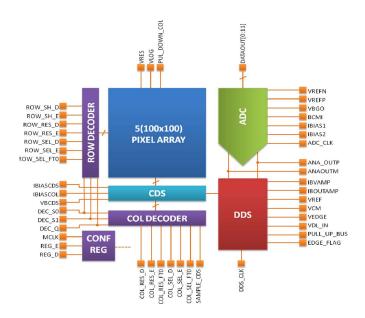
Fig. 3. Simplified block diagram of the camera.

or logarithmic, this correction is performed, respectively, on the whole signal chain or just on a part of it. In particular, when the pixel is in the reset condition, the level of V_{PH} is such that the active load is not working. This condition means that M2 and M3 are not involved in the signal path during the acquisition of the reset value; thus, their FPN contribution cannot be subtracted.

The sampling operation of the CDS block can be summarized as follows:

$$V_{SigCDSOut} = [(V_{ResPix} - V_{SigPix}) + V_{bCDS}] \times G_{CDS} \quad (7)$$

where $V_{SigCDSOut}$ is the output of the CDS, V_{ResPix} and V_{SigPix} are the reset and signal output of the pixel, respectively, V_{bCDS} is an external reference voltage, and G_{CDS} is the CDS gain.

Each CDS block is then reset to generate a reference value for the following DDS block. The reset output of the CDS is

$$V_{ResCDSOut} = V_{bCDS} \times G_{CDS}. \quad (8)$$

The following operation is the sequential selection of each CDS block by a column decoder. After the selection, the output value of each CDS is transferred to the DDS twice: one time for the signal and another time for the reset value. The DDS is a fully differential switched capacitor block that performs a subtraction between the signal and the reset value from each CDS, the addition of a threshold voltage (V_{REF}), and a multiplication by a gain factor (GAIN). Such a gain can be set by the user, ranging from 1 to 4, by changing the input capacitance of the switched capacitor circuit. The resulting DDS output is differential as described in the following relation:

$$V_{OutDDS\pm} = V_{CM} \pm GAIN$$
$$\times (V_{REF} - (V_{ResCDSOut} - V_{SigCDSOut})) \quad (9)$$

where $V_{OutDDS\pm}$ are the DDS outputs, and VCM is the common mode signal.
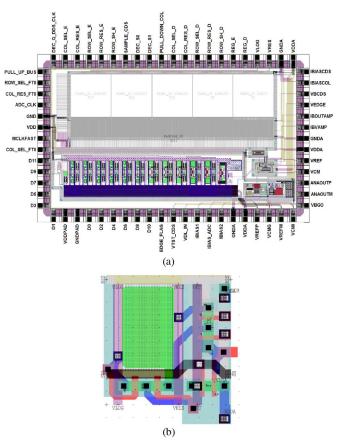

(a)

(b)

Fig. 4. Complete (a) imager and (b) pixel layout.

The DDS differential output signals are sent to a 12-b pipelined ADC [22] and digitized into 4096 levels. Therefore, each pixel is described by a 12-b word as follows:

$$ADCOUT = \frac{V_{OutDDS}^+ - V_{OutDDS}^-}{V_{REFP} - V_{REFN}} * 2^{11} \quad (10)$$

where V_{REFP} and V_{REFN} are the ADC reference voltages, and $ADCOUT$ is the ADC digital output word.

IV. EXPERIMENTAL RESULTS

The image sensor presented in this paper was fabricated in the standard 0.35-μm mixed-signal CMOS technology from ON-Semiconductors. The chip layout is shown in Fig. 4(a).

The die size is 6.36 mm $\times$ 3.68 mm, including test structures, more than five 100 $\times$ 100 pixel arrays, not described in this paper. Only the first 100 $\times$ 100 array based on a standard layout design [see Fig. 4(b)] was considered and characterized. Electro-optical tests were carried out on a dedicated electro-optical bench to characterize the imager performance. For this purpose, a custom system was developed (see Fig. 5) to interface the sensor with a personal computer (PC). The system consists of two boards. The first board (referred to as the "daughter board" in Fig. 5) is a custom board, particularly designed to interface the vision sensor with the second board (referred to as "mother board" in Fig. 5) through a couple of 50-pin stripes. The second board features a 100-Kgates field-programmable gate array (FPGA; Xilinx, Spartan). The code
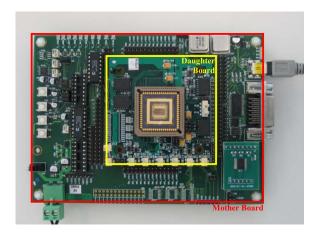
Fig. 5.   Customized test boards.

(a)

(b)

Fig. 6.   (a) Power responsivity and (b) SNR at different V_{LOG} and T_{INT} values over the whole LIPD range.

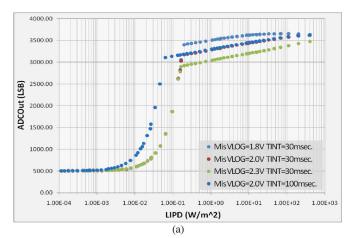that was loaded on the FPGA enables imager control and interfacing of the imager with a PC-based user console.

With regard to electro-optical characterization, the overall integration time was set to 30 and 100 ms, and the V_{LOG} reference ranged from 1 V to 3.3 V to assess the power responsivity modulation. The reference signals of the sensor were set to have an offset value of 500 LSBs, thus preventing downward saturation of the readout channel. This condition guarantees accurate sensitivity estimation, which measures the capability of the sensor to detect low LIPD. Note that sensitivity can be identified by the LIPD value, where SNR = 1 for the given configuration of the sensor parameters [6].

As shown in Fig. 6(a), a DR of 110 dB can be achieved over an effective number of bits of 11.5 by setting $T_{INT} = 30$ ms and $V_{LOG} = 2.3$ V. For this specific case, 11.2 b resolves the linear region of the sensor, thus covering 2.25 decades of irradiance (45 dB). The rest of the dynamics, i.e., 65 dB, which is equivalent to more than three decades, is logarithmically mapped over 9.2 b, with a significant decrease in resolution.

To test power responsivity modulation, V_{LOG} was set at three different values, i.e., 1.8, 2.0, and 2.3 V. As represented in Fig. 6(a), an increase in V_{LOG} results in a shift of the transition point from the linear to the logarithmic region in the power responsivity curve. Furthermore, when changing the V_{LOG} value from 1.8 V to 2.3 V, the resolution loss in the linear region is negligible if compared to the overall gain of one decade in the DR.

Note that the 110-dB power response limit is due to the measurement setup, which cannot provide the sensor with a LIPD over 10^3 W/m^2. This limit can theoretically be extended over 120 dB with a proper sensor setting, as detailed later on in this paper. Furthermore, pixel sensitivity can be improved by increasing the integration time, similar to a standard linear active pixel sensor (APS). This feature was both modeled (see Fig. 2) and experimentally assessed by setting the integration time up to 100 ms, thus obtaining an improvement in sensitivity by a factor of 30.

Noise performance of the sensor was extracted from experimental results as a percentage of the signal range. The average FPN value was measured at different LIPD levels as the standard deviation of pixel values over an image acquired without a focusing lens on top of the chip. To exclude pixel
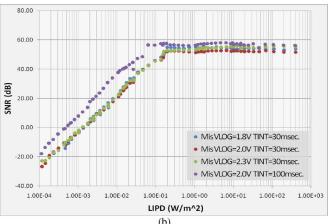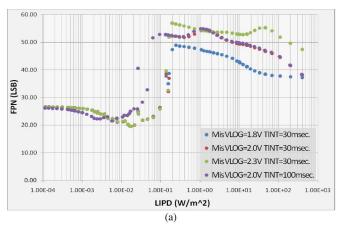
noise (PN), the standard deviation was calculated over an image that results from the average of 100 acquisitions at constant environmental and setting conditions. The resulting value for FPN is 0.83% in the linear region and 1.37% in the logarithmic region [see Fig. 7(a)]. PN was measured over the whole LIPD range as the standard deviation over 100 pixel acquisitions taken at constant environmental and setting conditions. To avoid FPN contribution, each value was taken as the average pixel over a whole image. The resulting value for PN is less than 0.22% of the whole signal range [see Fig. 7(b)].

The measured SNR, defined as the signal over the PN (in decibels), is plotted in Fig. 6(b) for the entire dynamic range (DR). Note that variations in V_{LOG} do not affect the SNR response. Furthermore, there is no appreciable decrease in the SNR curve for strong incident light, thus potentially allowing us to achieve a maximum DR larger than 120 dB.

Examples of *ex vivo* biological images of a porcine stomach, acquired with the described chip, are shown in Fig. 8. The same image was acquired with different V_{LOG} levels to show the increasing number of details that can be obtained by tuning V_{LOG}. To quantify this variation, the histogram of each image is included. The additional information content that can be recovered by increasing V_{LOG} is highlighted with a circle. Note that no processing was applied to the images shown in Fig. 8. Residual FPN in the high-light power region is 1.37% of the full signal range, i.e., four times lower than with a standard
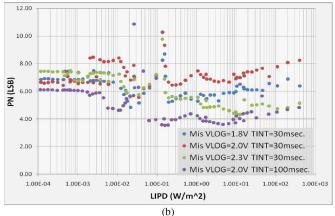
Fig. 7. (a) FPN and (b) PN at different V_{LOG} and T_{INT} values over the whole LIPD range.

logarithmic pixel [23]. The main performance of the image sensor is summarized in Table I.

The power responsivity results were compared with the model presented in Section II. Parameters that cannot directly be measured on chip, e.g., the photodiode capacitance, were tuned around values that were calculated considering the 0.35-μm ON-Semiconductor process parameters (e.g., $C_{IN} = 16$ fF and $i_D = 52$ fA). Fig. 9 shows a good fit between the model and the measurements, both in the logarithmic and the linear regions.

This fit was quantified as percentage error for each LIPD step and is plotted in Fig. 10. The average percentage error over the LIPD range, excluding the saturated regions, is around 0.8% for all the considered sensor configurations, with a peak in the transition region.

Once model output reliability has been demonstrated, the DR that may be achieved by the sensor can further be discussed. As reported in Fig. 11, by setting $V_{LOG} = 2.3$ V, the model predicts a LIPD saturation of 4×10^6, thus achieving more than 120 dB in the DR. This result is further supported by the aforementioned SNR stability at high LIPD.

V. CONCLUSION

A novel linear–logarithmic pixel for intraframe HDR image sensor, featuring a 12-b digital output, has been presented. This pixel configuration was integrated in a 100×100 pixel
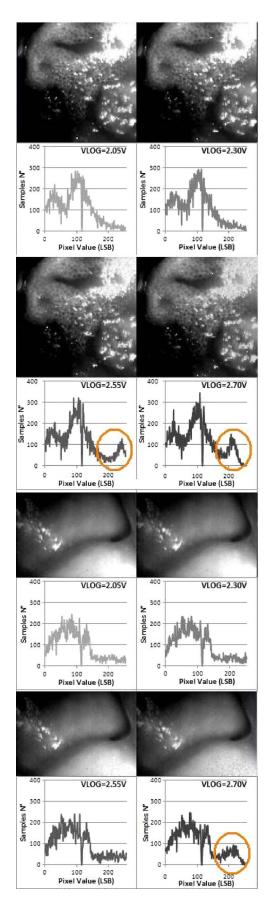

Fig. 8. Comparison between *ex vivo* images of a porcine stomach with different dynamic ranges, from low ($V_{LOG} = 2.0$ V) to high ($V_{LOG} = 2.70$ V) threshold values.

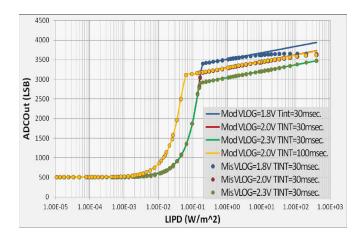| Parameter	Value
Technology	0.35μm, 3.3V CMOS (2P-4M)
Pixel pitch	9.4 μm×9.4 μm
Array size	100×100 pixels
Chip size	6.36 mm×3.68 mm
Operating supply current	4 mA (Digital part @ 30fps)
	32 mA (Analog part @ 30fps)
Fill factor	30%
Sensor output	12 bit digital output
Fullwell Capacitance	170000 e- @27°C
FPN(linear, logarithmic reg.)	0.83%, 1.37% @ 27°C
	1400, 2300 e- @27°C
Temporal Noise (linear, logarithmic reg.)	< 0.22% @ 27°C
	<370 e- @27°C
Dynamic range	112 dB
SNR(max)	55 dB @ 27°C
Dark Signal	0.22% (370 e-) (of saturation signal at room temperature)

Fig. 9. Modeled and experimental power responsivity of the linear–logarithmic pixel at different V_{LOG} and T_{INT} values over the whole LIPD range.
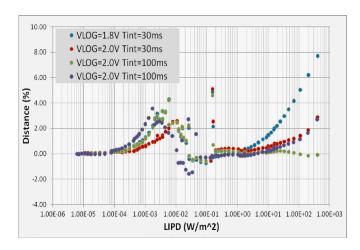

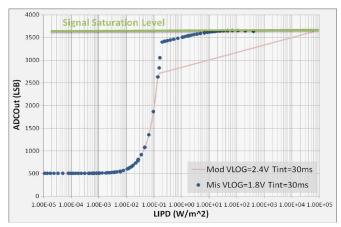Fig. 10. Percentage error over the LIPD range in the fit of the measured results by the model for different V_{LOG} and T_{INT}.

Fig. 11. Percentage error over the LIPD range in the fit of the measured results by the model for different V_{LOG} and T_{INT}.

array within a monochrome imager. A DR over 110 dB was experimentally measured, whereas an extension over 120 dB, not measurable due to measurement setup limitations, is expected on account of the modeling results and SNR stability at high LIPD. Measurement results show good PN (0.22% rms) and FPN (0.83–1.37%) performance, both in the linear and the logarithmic regions. Furthermore, the DR and, accordingly, the resolution of the power responsivity curve can simply be adjusted by tuning the point of transition between the linear and the logarithmic domains through the setting of an analog reference signal (i.e., V_{LOG}).

A behavioral model of the linear–logarithmic pixel was presented and compared with the experimental results. The average percentage error in the fit between experimental and theoretical data was 0.8%. Given such consistency, the model can be used to estimate the DR with different settings of the reference signals or to extrapolate specific device parameters from experimental data (e.g., the photodiode capacitance and the dark current), which would otherwise be impossible to experimentally quantify.

The sensor was tested by acquiring images from an *ex vivo* porcine stomach. Due to the sensor's ability to be self referential by changing V_{LOG} and, accordingly, the DR, the efficiency of an HDR response in comparison with a standard DR one was proven. The main result consists of additional details in the HDR image if compared to the standard DR one. In endoscopic imaging, HDR is useful in case of high reflective regions, mainly in correspondence of wet mucosa. In the case of the presented pixel, these regions are mapped in the logarithmically extended dynamic, thus avoiding saturation of the scene and providing better detail to the user.

To complete the characterization of the pixel, a spectral responsivity measurement will be performed as the next step to gather information about the spectral performance and the quantum efficiency.

The presented HDR pixel technology will be implemented in a second prototype with extended resolution. Filters will be added to obtain a color image stream, which is of paramount importance in the targeted biomedical application.

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